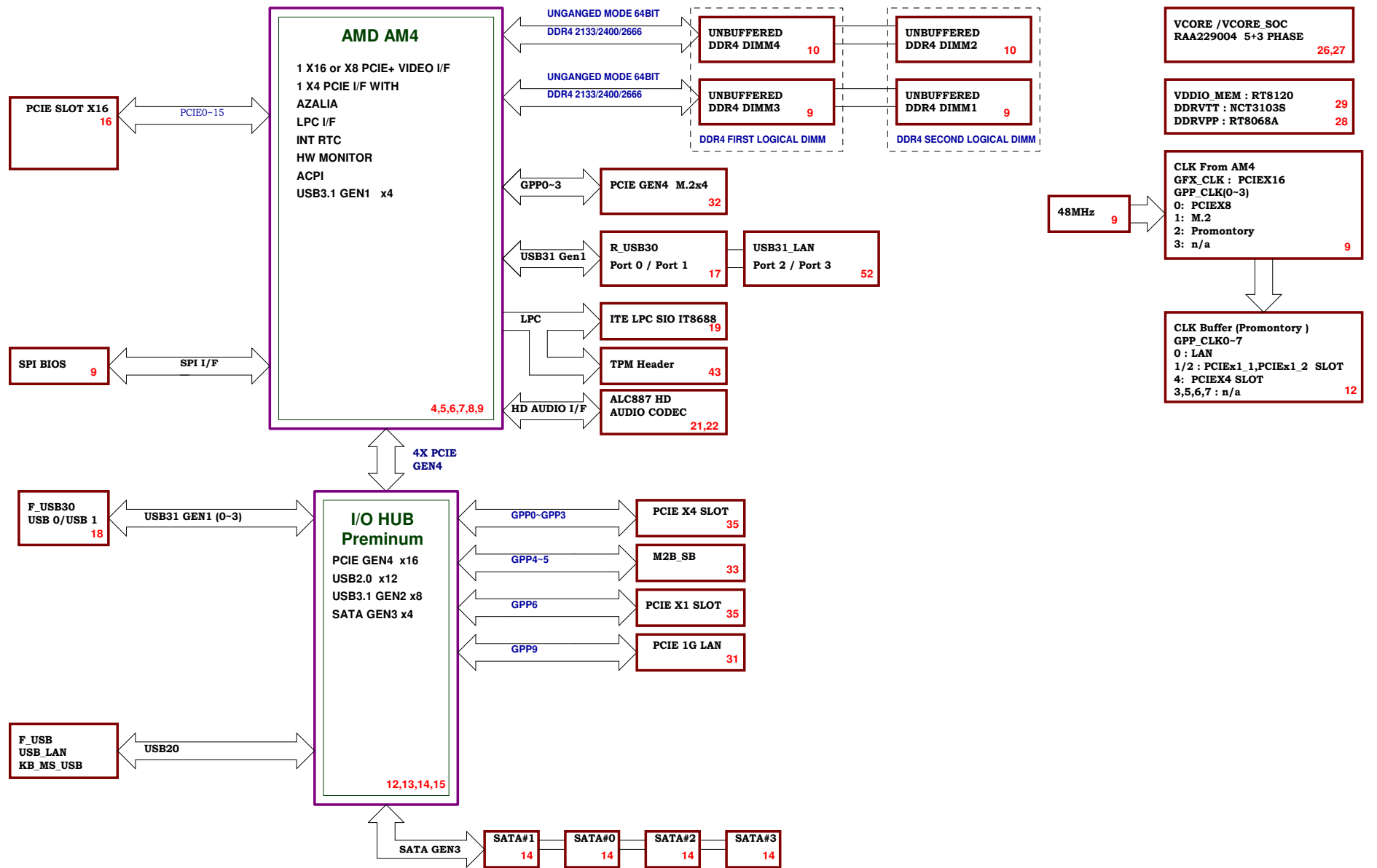


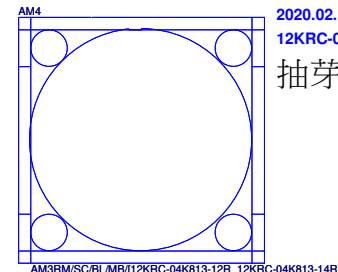
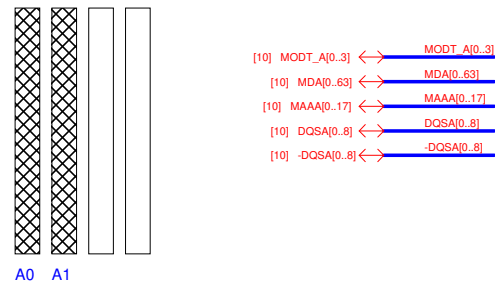
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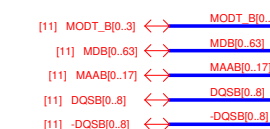
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MEM CHA



2020.02.17
12KRC-04K813-12R/14R
抽芽式



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Title: **APU DDR4**

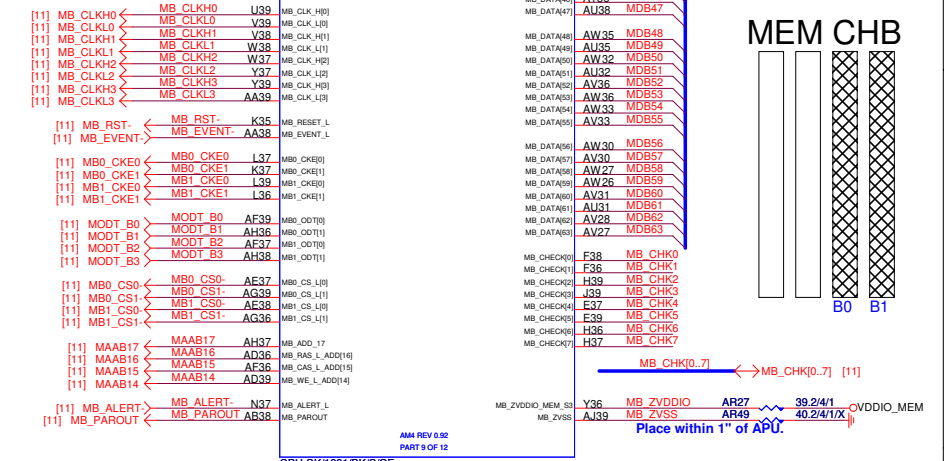
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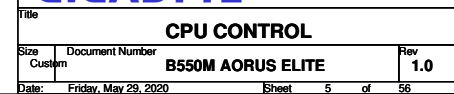
Date: Wednesday, April 22, 2020 Sheet 4 of 56

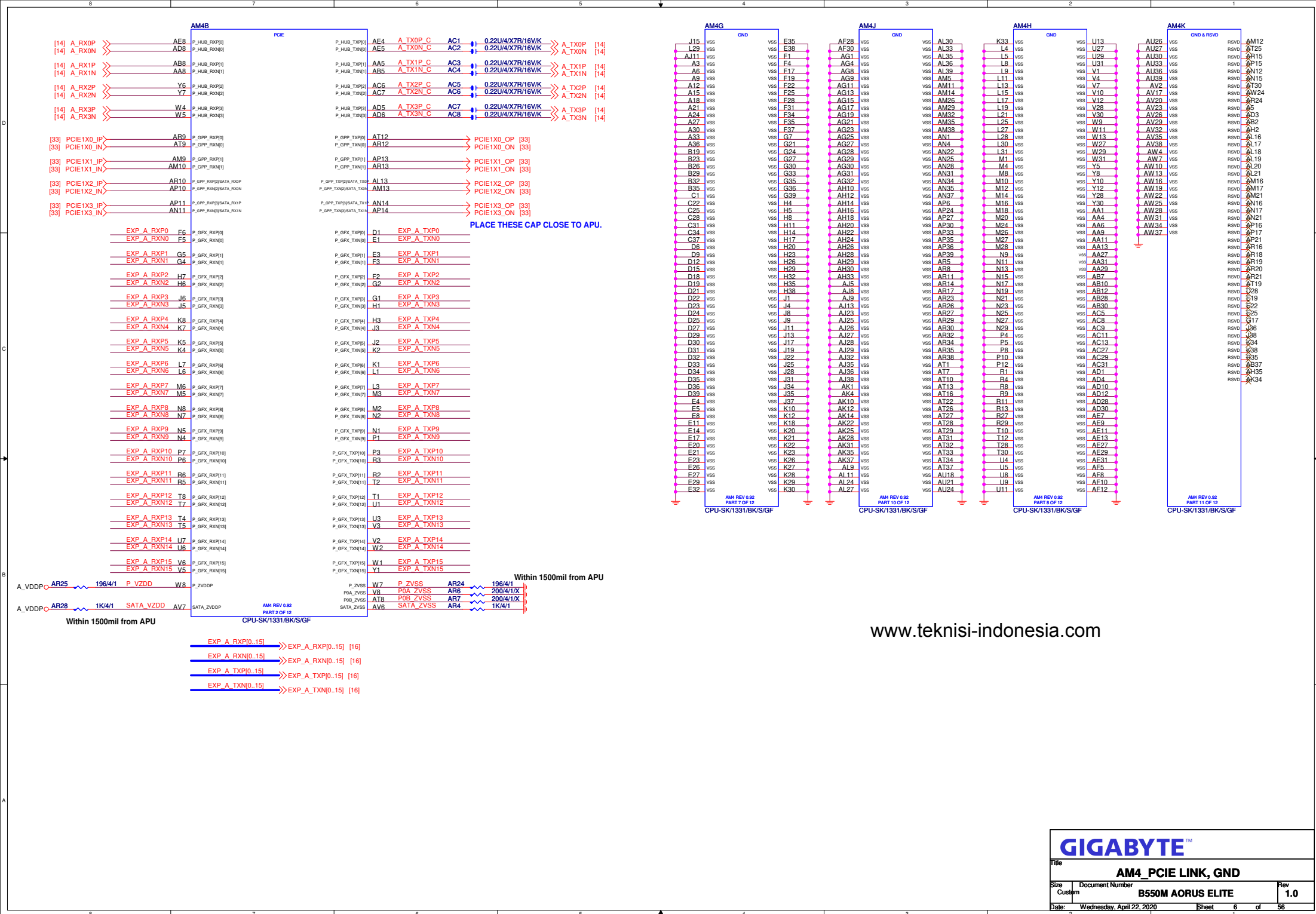
A0 A1

B0 B1

MEM CHB

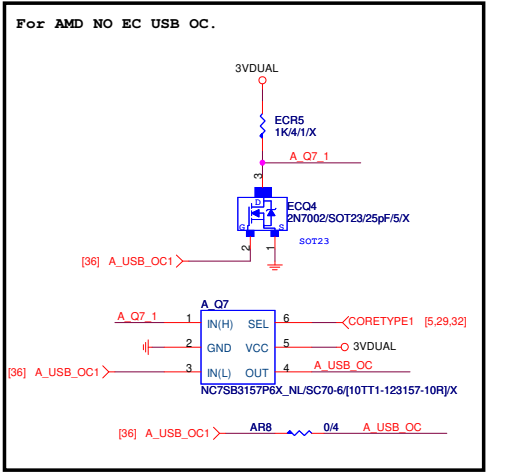
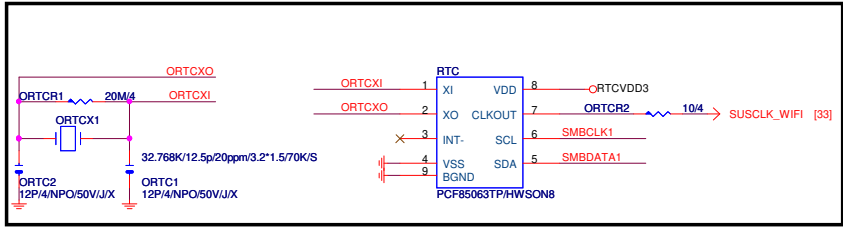
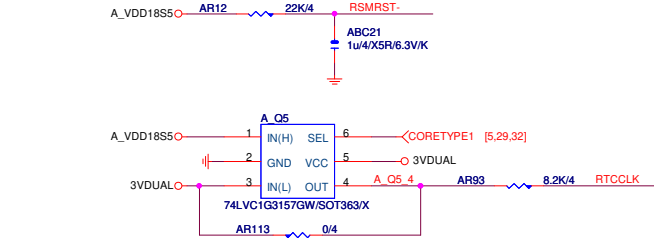
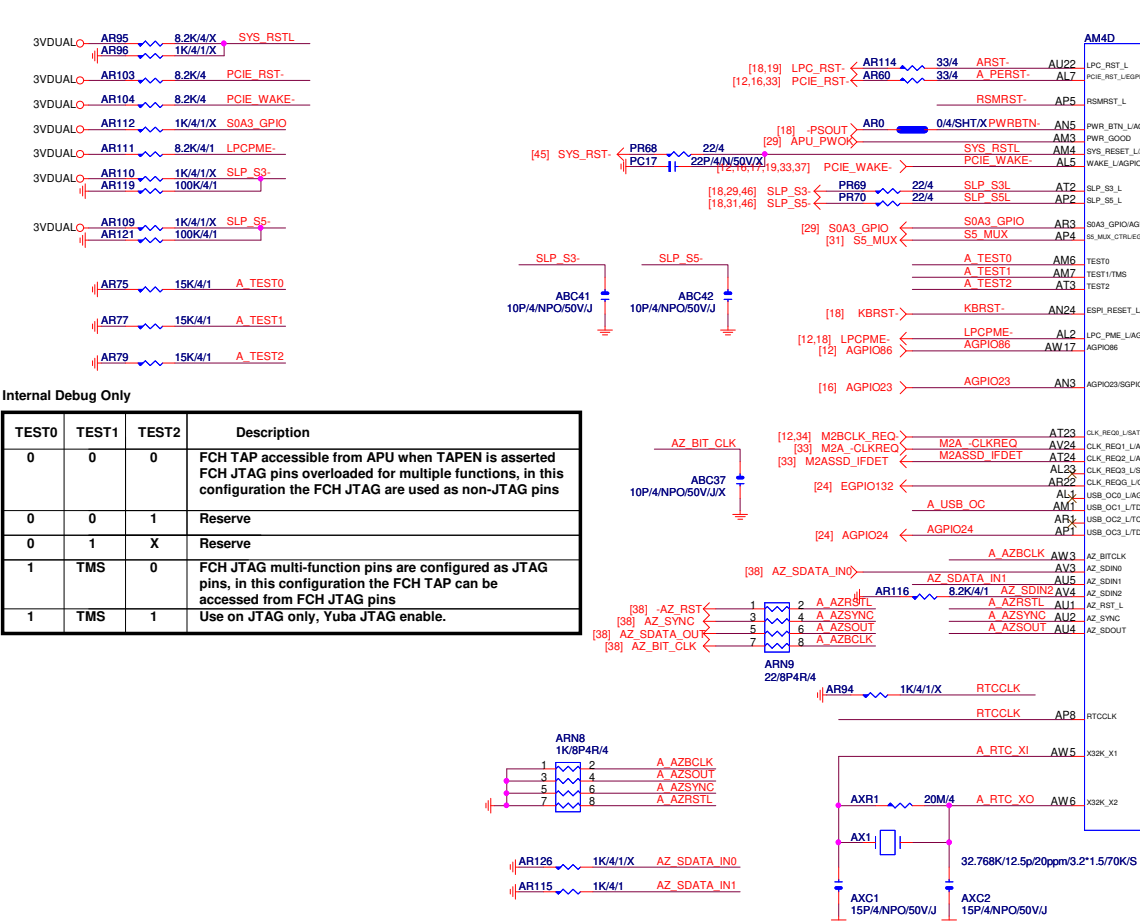






Internal Debug Only

TEST0	TEST1	TEST2	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserve
0	1	X	Reserve
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on JTAG only, Yuba JTAG enable.

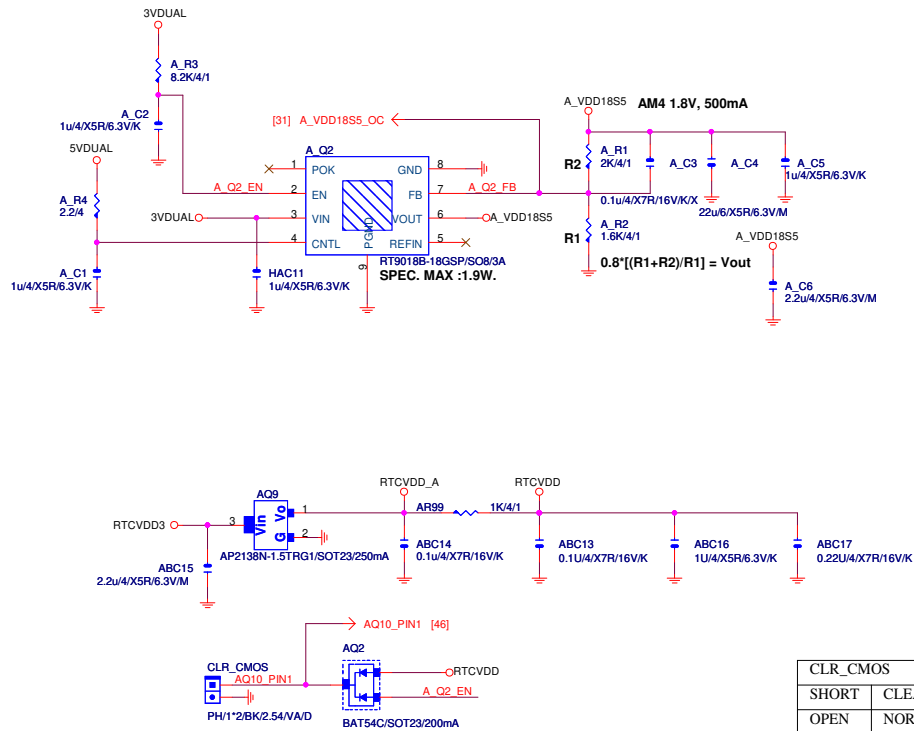
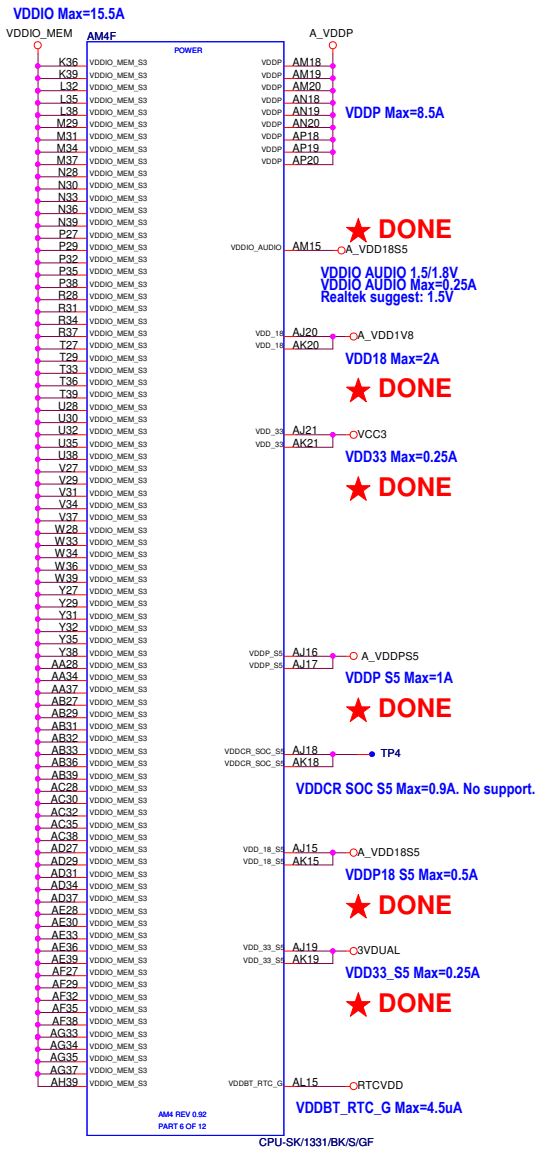


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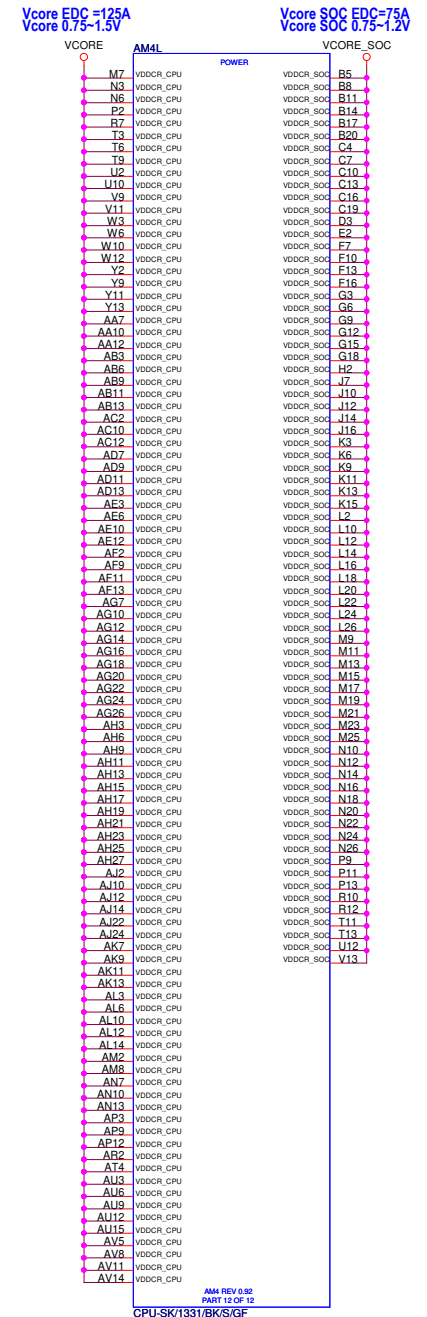
AM4 MISC

Size Custom Document Number B550M AORUS ELITE Rev 1.0

Date: Wednesday, April 22, 2020 Sheet 7 of 56



CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL
NOT ADD ICT FOR RTCVDD PIN	

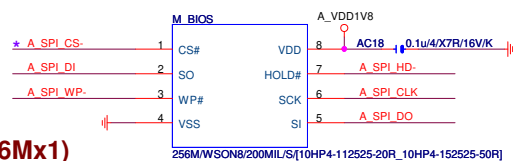
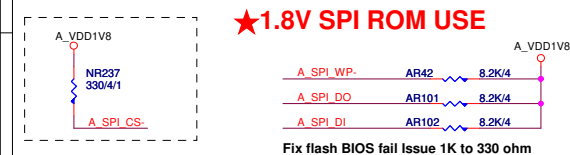
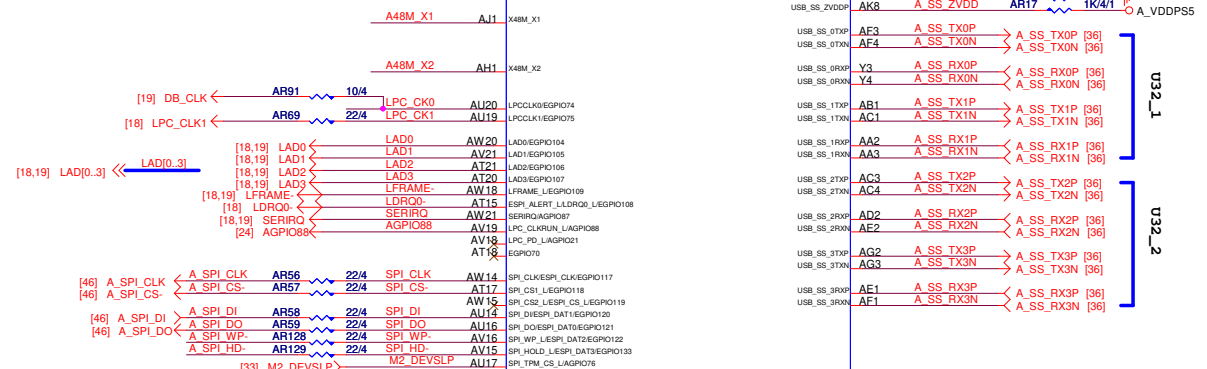
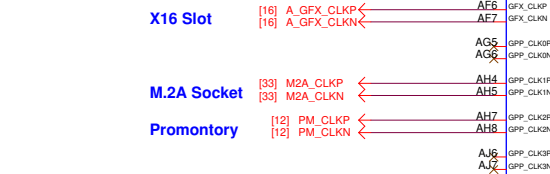
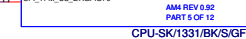
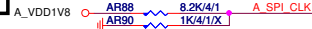


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Title CPU POWER & GND			
Size	Document Number	Rev	
Custom	B550M AORUS ELITE	1.0	
Date:	Friday, May 08, 2020	Sheet	8 of 56

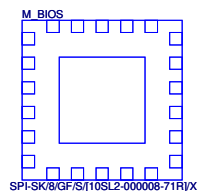


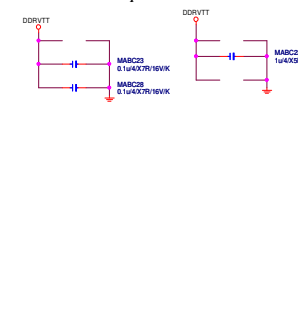
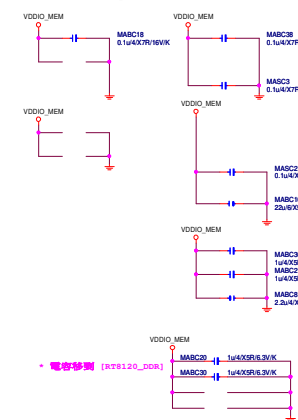
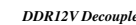
	SPI_CLK	LFRAME-	SYS_RST-	LPC_CLK0	LPC_CLK1
PULL HIGH	Internal clock mode	SPI ROM	Normal reset mode	PSP modify SPI page reg bits[24:24]	Use 48MHz crystal clock
PULL LOW	Extal clock mode	LPC ROM	Short reset mode	PSP not modify SPI page reg bits[24:24]	Use 100MHz extl clock input.

Bule: default

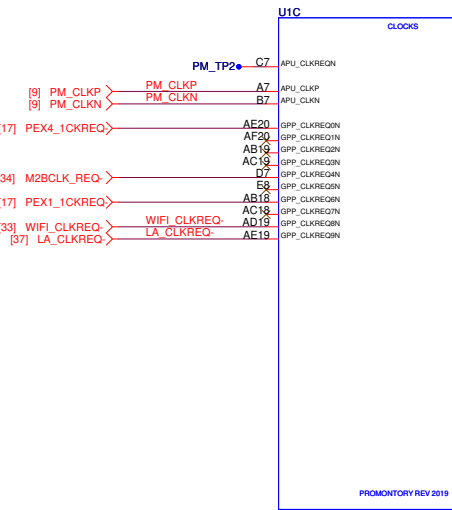


Single (256Mx1)
Layout colay 128Mx1

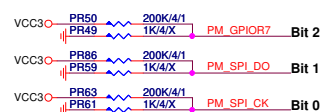
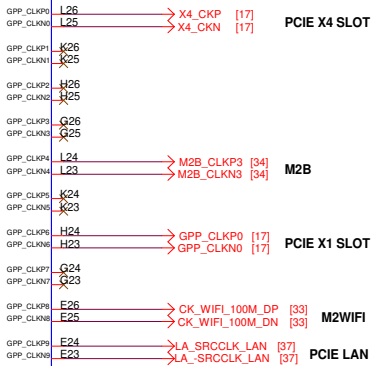




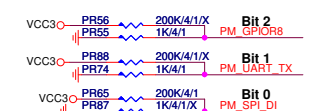
teknisi-indonesia.com



R0.2 Update
CLK & CLK REQ 需與PCIE Port mapping



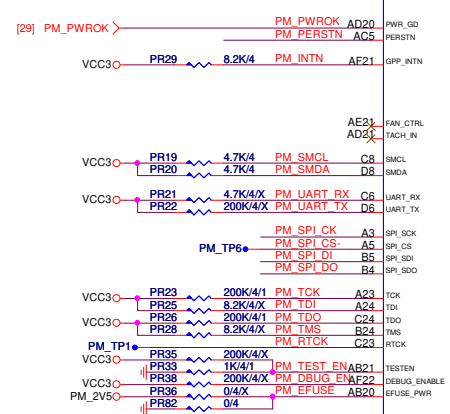
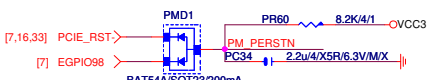
Bit 2	Bit 1	Bit 0	GPP Group 0 (Lanes 3:0)
0	0	0	4 PCIe x1
0	0	1	2 PCIe x1 + 1 PCIe x2
0	1	0	1 PCIe x2 + 2 PCIe x1
0	1	1	1 PCIe x2 + 1 PCIe x2
1	1	1	1 PCIe x4
Others: Reserved			



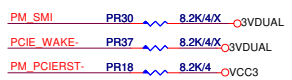
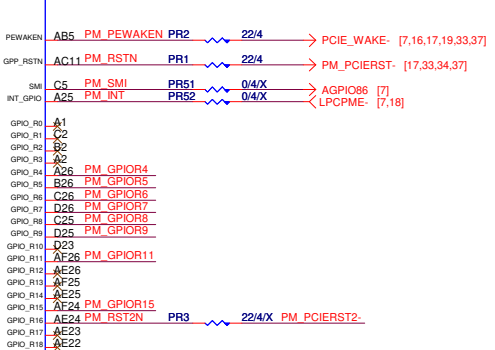
Bit 2	Bit 1	Bit 0	GPP Group 1 (Lanes 7:4)
0	0	0	4 PCIe x1
0	0	1	2 PCIe x1 + 1 PCIe x2
0	1	0	1 PCIe x2 + 2 PCIe x1
0	1	1	1 PCIe x2 + 1 PCIe x2
1	1	1	1 PCIe x4
Others: Reserved			



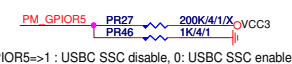
GPP Group 2 (Lan 8:9)=>1: PCIe x2, 0: 2 PCIe x1



PR71 1K/4/1 PM_DEBUG_EN
PR79 1K/4/X PM_TCK
PR80 1K/4/X PM_TDO
TESTEN=>1:Test Mode, 0:Function mode.
DEBUG=>1:Debug Mode, 0:Function mode.



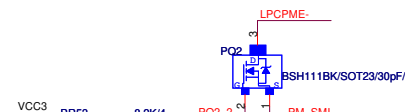
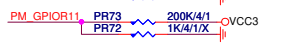
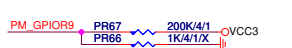
PM_GPIOR4: GPP clock source from APU_CLKP/N;
0: GPP clock source from Crystal.



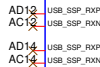
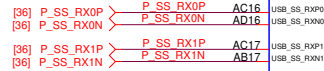
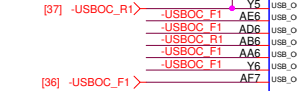
GPIOR5=>1: USB SSC disable, 0: USB SSC enable



GPIOR6=>1: SATA SSC disable, 0: SATA SSC enable

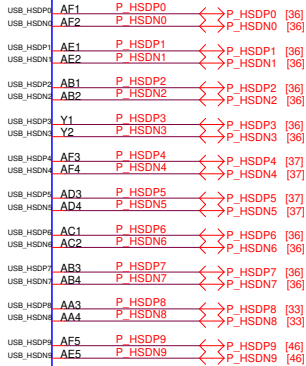


USB port power control 9:0
(VCC3). Output.



PROMONTORY REV 2019 218-0891014-00/S

USB32G2	USB20	USB_OC
0	0	0
1	1	1
USB32G1		
0	2	2
1	3	3
	4	4
	5	5
	6	6
	7	7
	8	7
	9	7



KB_MS_USB OK

KB_MS_USB OK

F_USB30 OK

F_USB30 OK

LAN_USB OK

LAN_USB OK

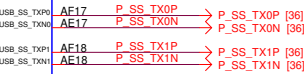
F_USB20 OK

F_USB20 OK

M2 WIFI OK

MCU OK

USB 3.1 Gen 1



HSD 2 F_USB30 OK

HSD 3 F_USB30 OK

USB 3.1 Gen 2



HSD 0

HSD 1

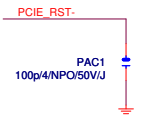
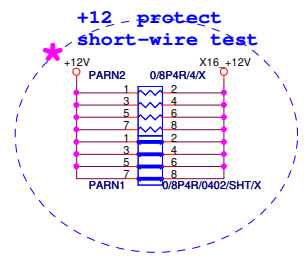
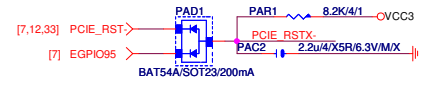
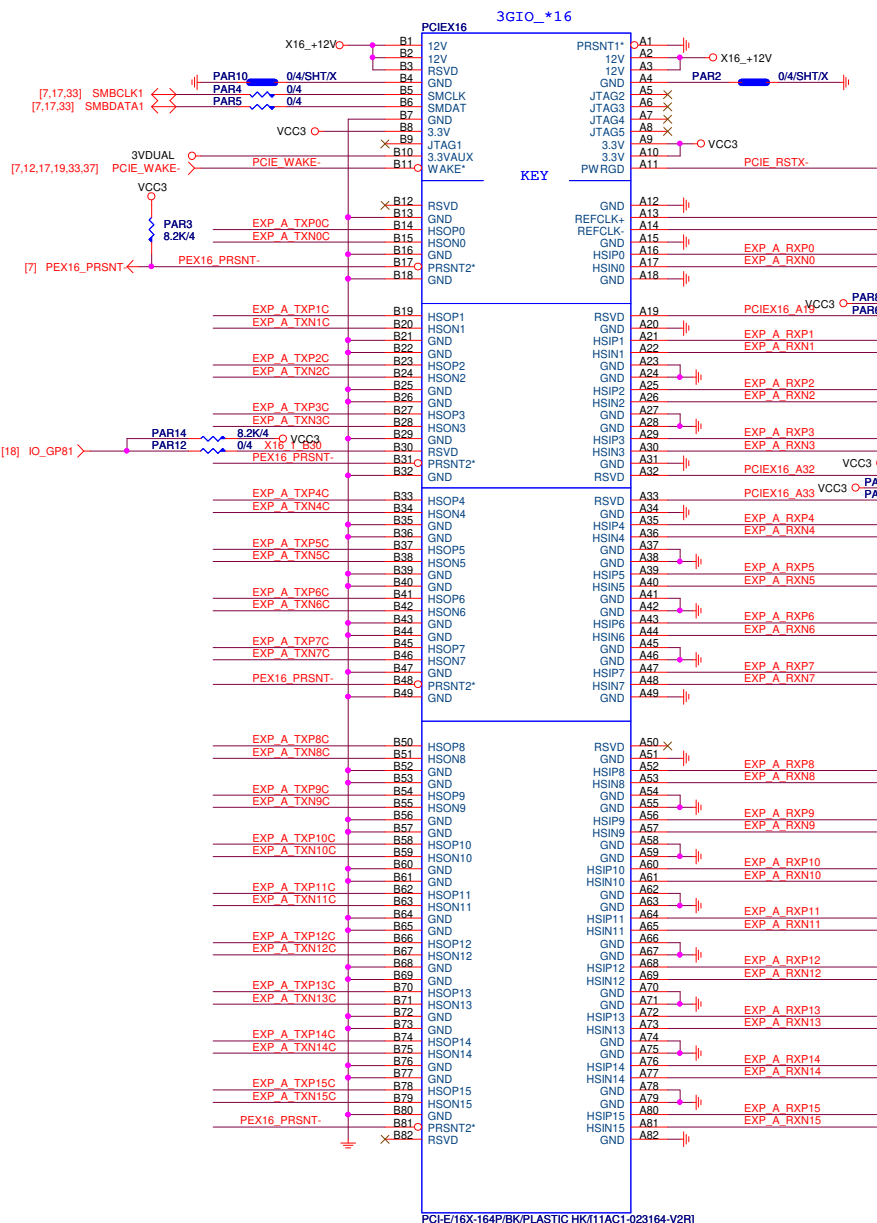
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ANS: 7967042

Title PM USB

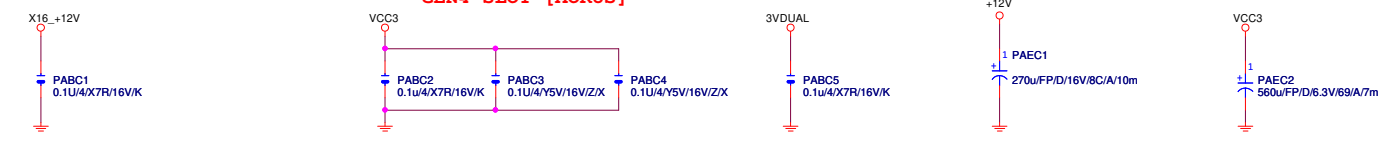
Size Custom Document Number B550M AORUS ELITE Rev 1.0

Date: Thursday, June 18, 2020 Sheet 13 of 56



EXP A TXP0	PAC4	0.22u/4/X5R/6.3V/K	EXP A TXP0C
EXP A TXN0	PAC5	0.22u/4/X5R/6.3V/K	EXP A TXN0C
EXP A TXP1	PAC6	0.22u/4/X5R/6.3V/K	EXP A TXP1C
EXP A TXN1	PAC7	0.22u/4/X5R/6.3V/K	EXP A TXN1C
EXP A TXP2	PAC8	0.22u/4/X5R/6.3V/K	EXP A TXP2C
EXP A TXN2	PAC9	0.22u/4/X5R/6.3V/K	EXP A TXN2C
EXP A TXP3	PAC10	0.22u/4/X5R/6.3V/K	EXP A TXP3C
EXP A TXN3	PAC11	0.22u/4/X5R/6.3V/K	EXP A TXN3C
EXP A TXP4	PAC12	0.22u/4/X5R/6.3V/K	EXP A TXP4C
EXP A TXN4	PAC13	0.22u/4/X5R/6.3V/K	EXP A TXN4C
EXP A TXP5	PAC14	0.22u/4/X5R/6.3V/K	EXP A TXP5C
EXP A TXN5	PAC15	0.22u/4/X5R/6.3V/K	EXP A TXN5C
EXP A TXP6	PAC16	0.22u/4/X5R/6.3V/K	EXP A TXP6C
EXP A TXN6	PAC17	0.22u/4/X5R/6.3V/K	EXP A TXN6C
EXP A TXP7	PAC18	0.22u/4/X5R/6.3V/K	EXP A TXP7C
EXP A TXN7	PAC19	0.22u/4/X5R/6.3V/K	EXP A TXN7C
EXP A TXP8	PAC20	0.22u/4/X5R/6.3V/K	EXP A TXP8C
EXP A TXN8	PAC21	0.22u/4/X5R/6.3V/K	EXP A TXN8C
EXP A TXP9	PAC22	0.22u/4/X5R/6.3V/K	EXP A TXP9C
EXP A TXN9	PAC23	0.22u/4/X5R/6.3V/K	EXP A TXN9C
EXP A TXP10	PAC24	0.22u/4/X5R/6.3V/K	EXP A TXP10C
EXP A TXN10	PAC25	0.22u/4/X5R/6.3V/K	EXP A TXN10C
EXP A TXP11	PAC26	0.22u/4/X5R/6.3V/K	EXP A TXP11C
EXP A TXN11	PAC27	0.22u/4/X5R/6.3V/K	EXP A TXN11C
EXP A TXP12	PAC28	0.22u/4/X5R/6.3V/K	EXP A TXP12C
EXP A TXN12	PAC29	0.22u/4/X5R/6.3V/K	EXP A TXN12C
EXP A TXP13	PAC30	0.22u/4/X5R/6.3V/K	EXP A TXP13C
EXP A TXN13	PAC31	0.22u/4/X5R/6.3V/K	EXP A TXN13C
EXP A TXP14	PAC32	0.22u/4/X5R/6.3V/K	EXP A TXP14C
EXP A TXN14	PAC33	0.22u/4/X5R/6.3V/K	EXP A TXN14C
EXP A TXP15	PAC34	0.22u/4/X5R/6.3V/K	EXP A TXP15C
EXP A TXN15	PAC35	0.22u/4/X5R/6.3V/K	EXP A TXN15C

EXP A RXP[0..15] >>> EXP_A_RXP[0..15] [6]
EXP A RXN[0..15] >>> EXP_A_RXN[0..15] [6]
EXP A TXP[0..15] >>> EXP_A_TXP[0..15] [6]
EXP A TXN[0..15] >>> EXP_A_TXN[0..15] [6]

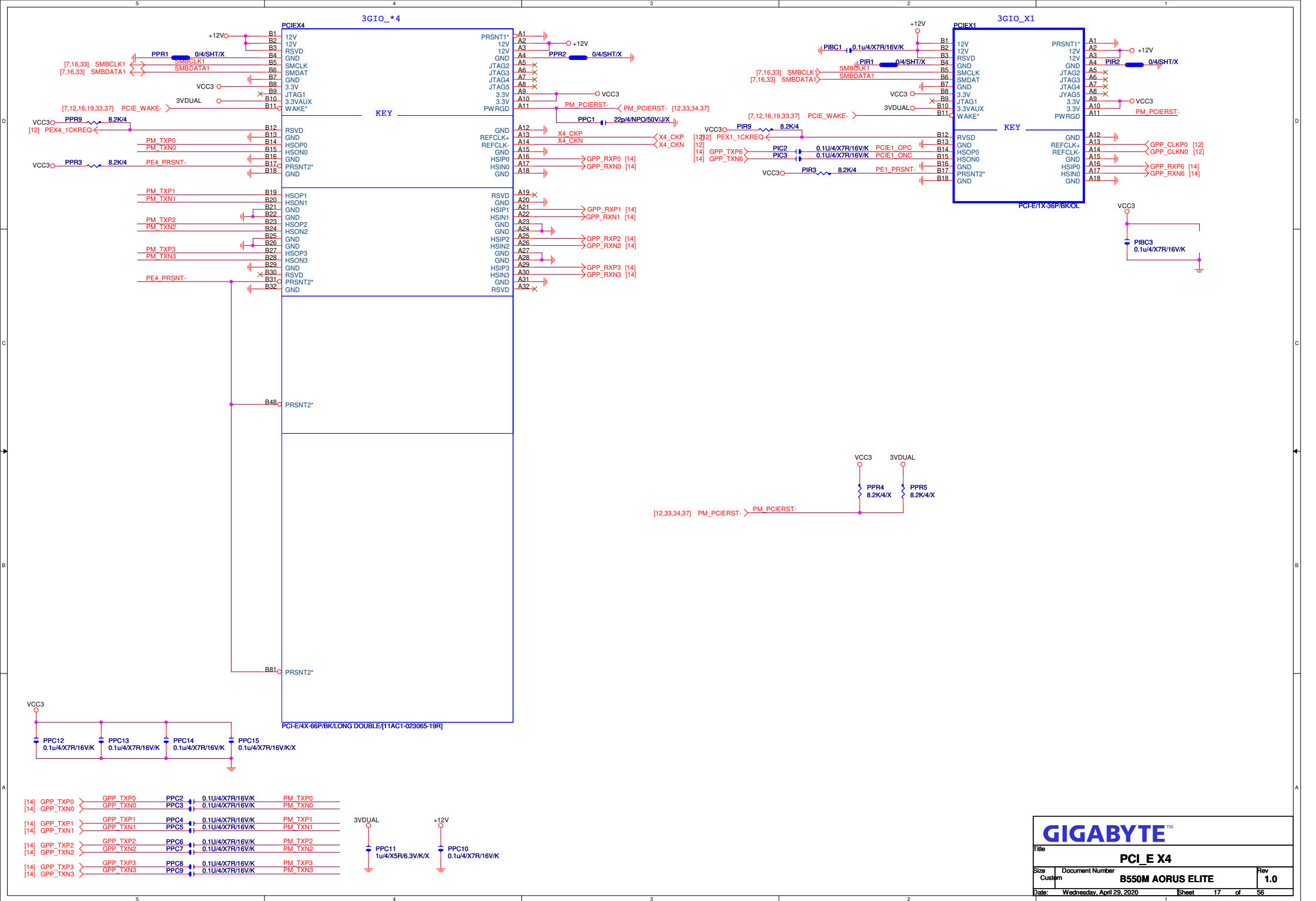


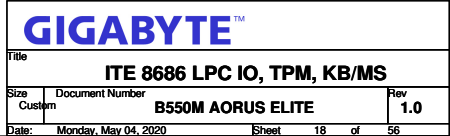
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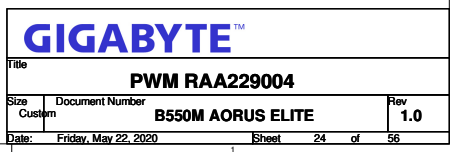
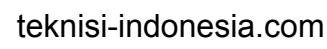
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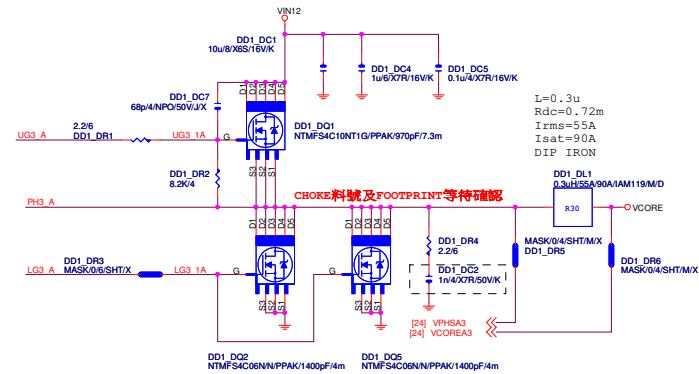
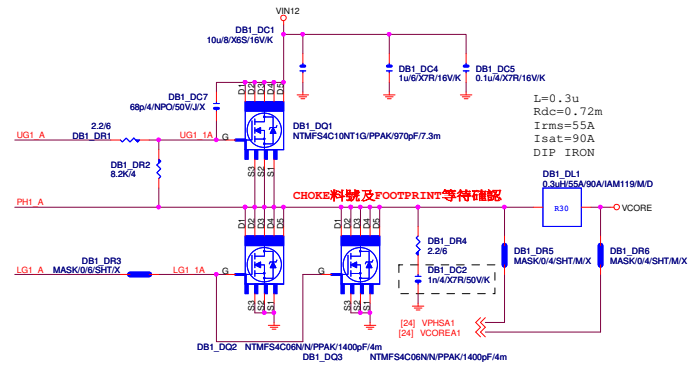
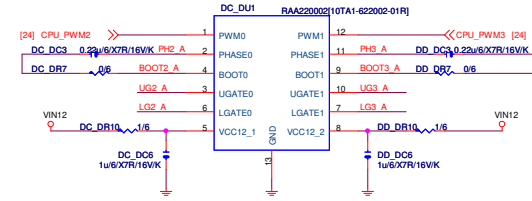
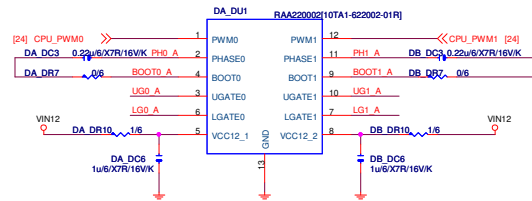
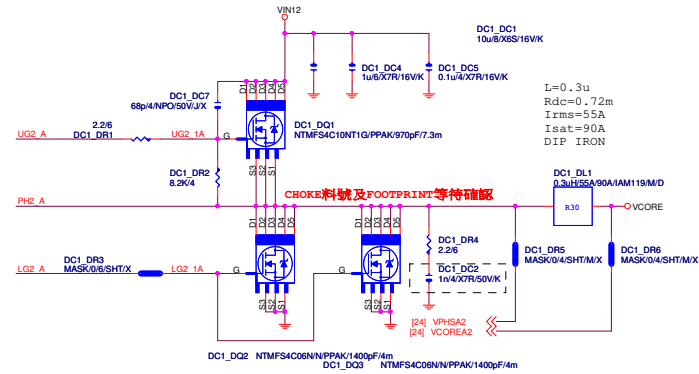
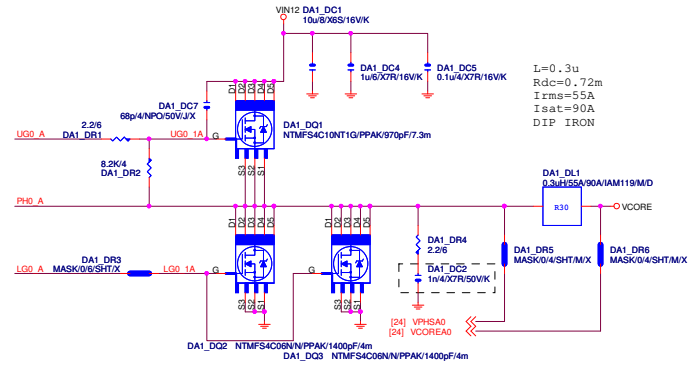
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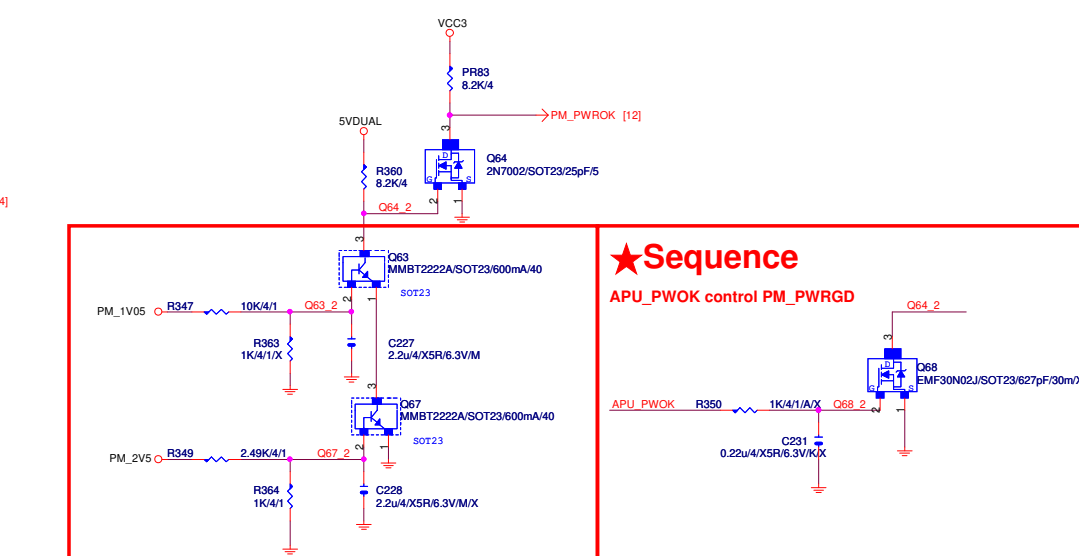
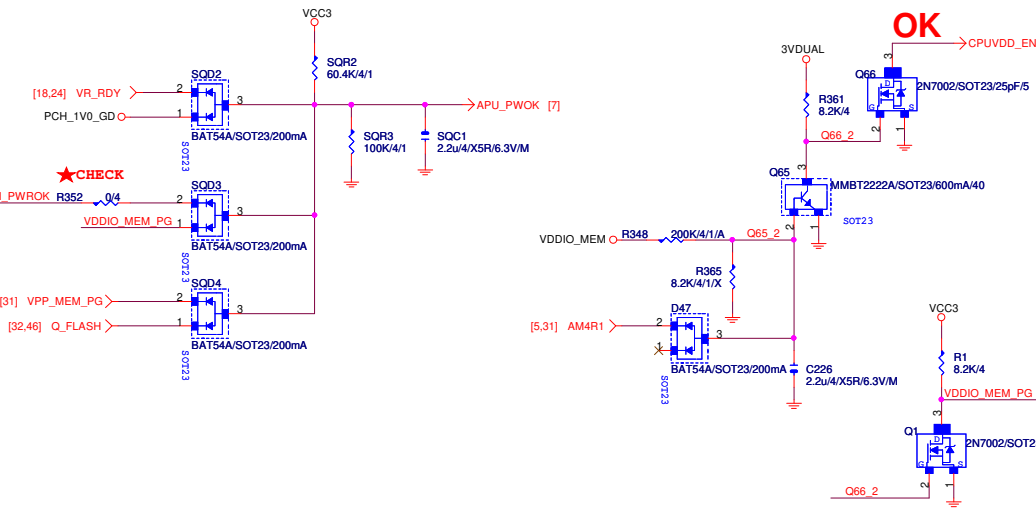
Date: Friday, May 08, 2020 Sheet: 16 of 56

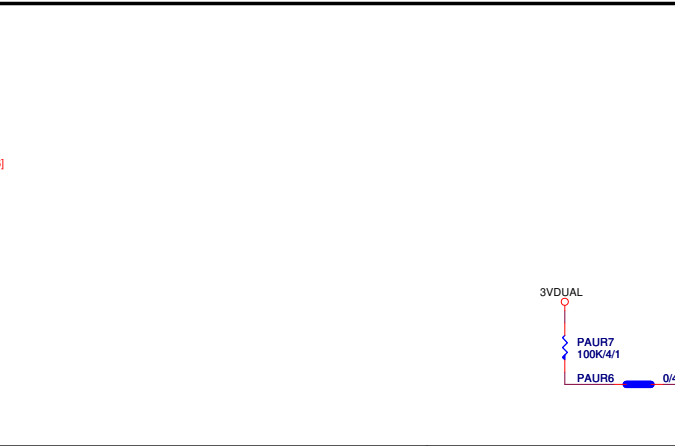
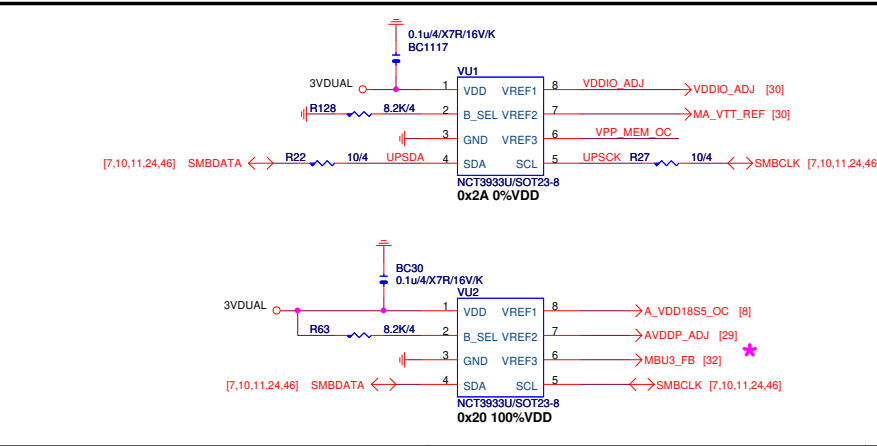
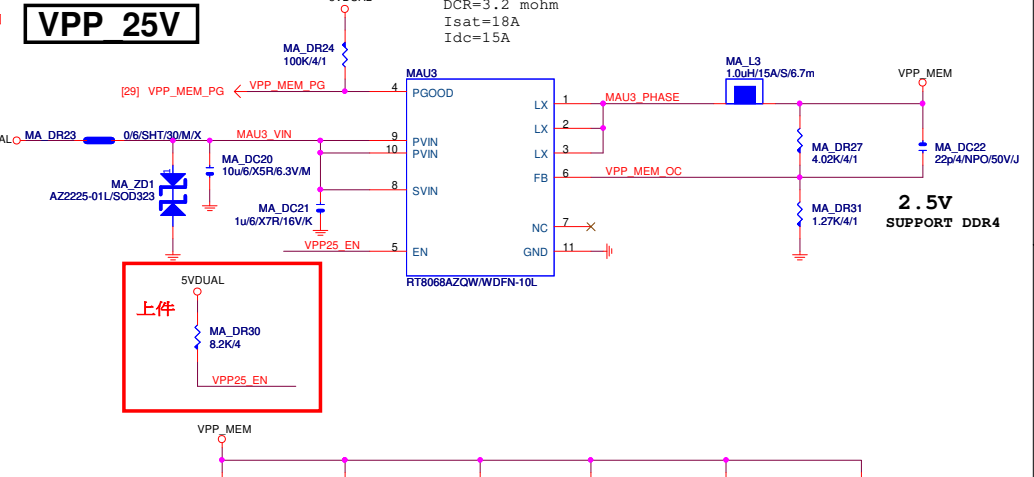
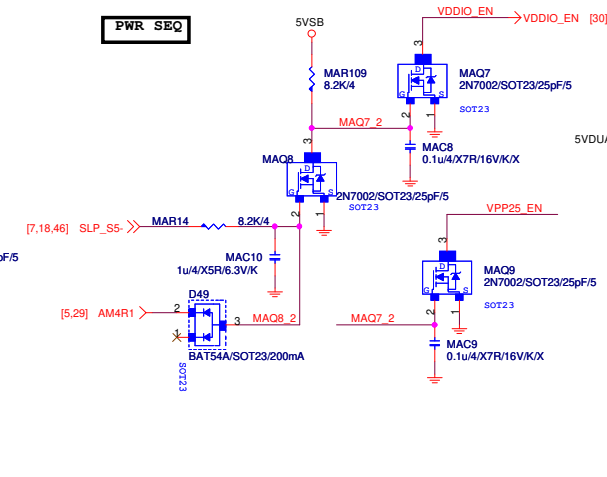
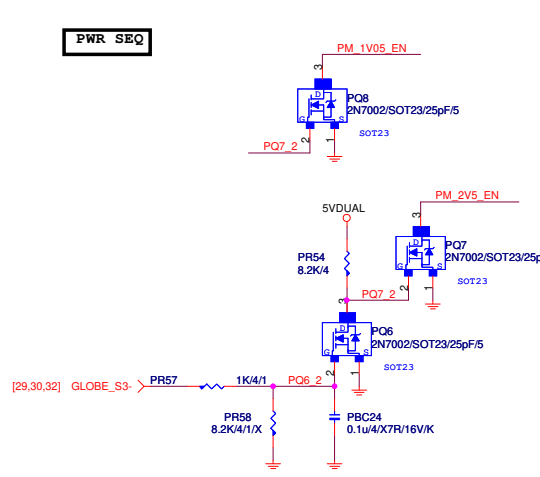
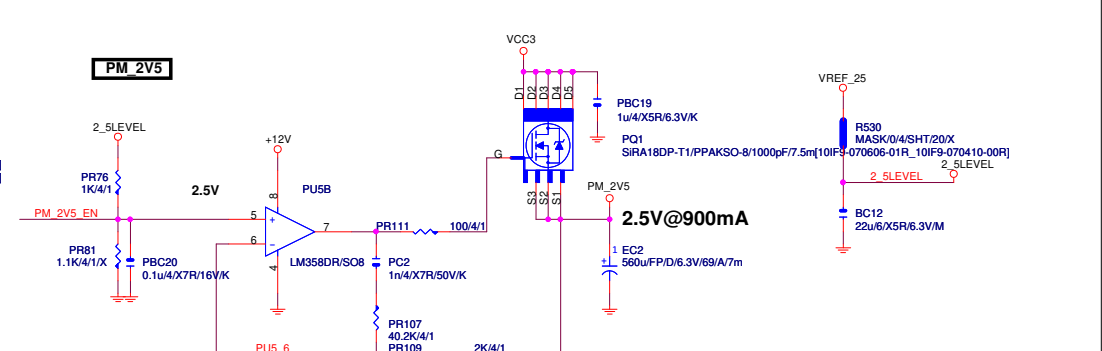
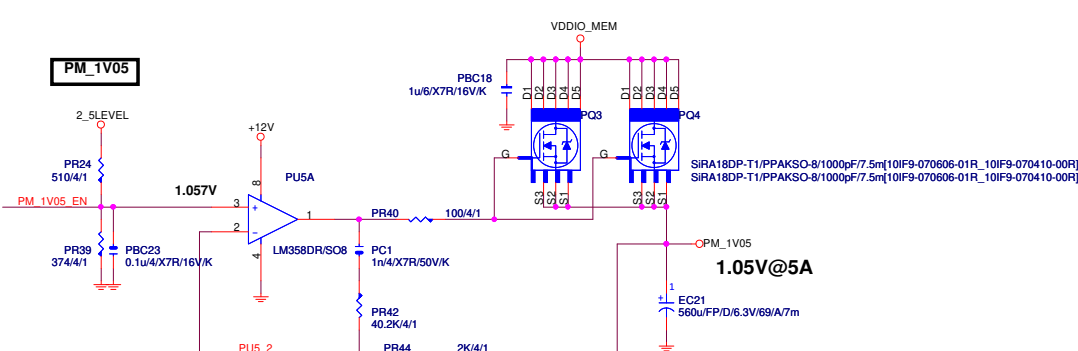












Address	0x2A	0x28	0x26	0x24	0x22	0x20
R1 (kΩ)	open	3.9	3	2.2	1.3	10
R2 (kΩ)	10	1.3	2.2	3	3.9	open
ADD_SEL Voltage (% of VCC)	0	25	42	58	75	100

Table1. Recommended Slave Address Setting

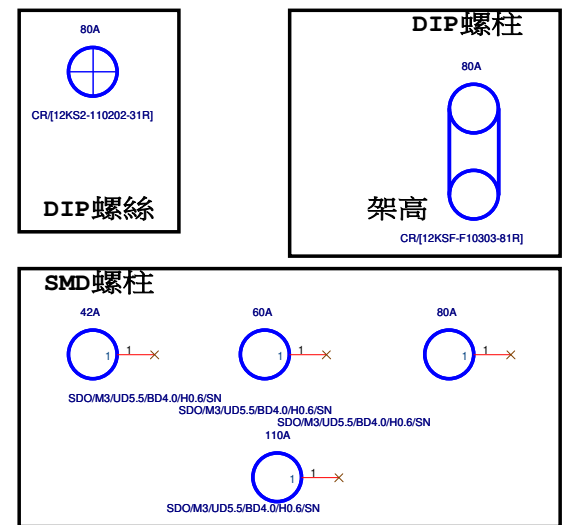
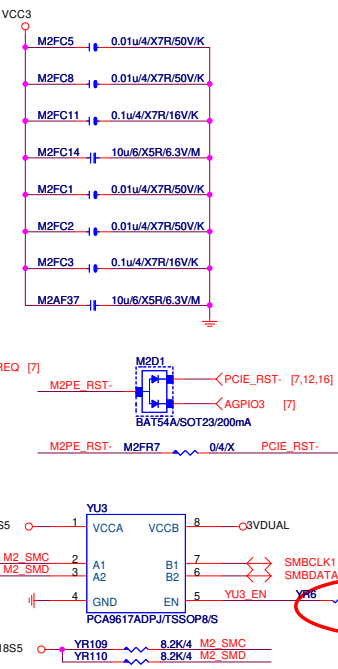
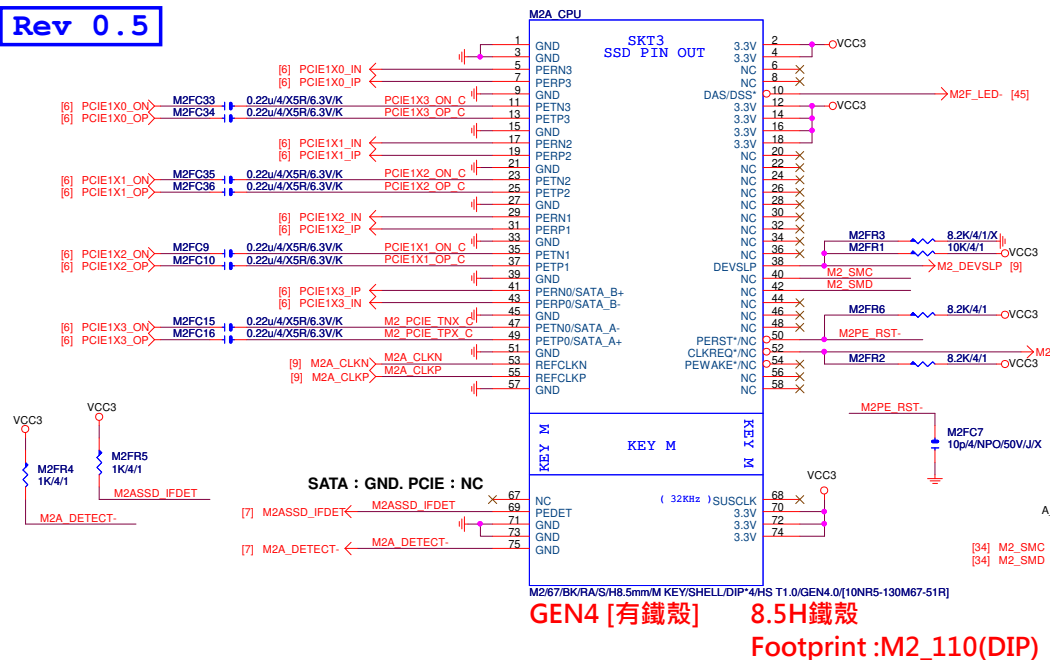
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Title: **VPP MEM**

Size: Custom Document Number: **B550M AORUS ELITE** Rev: **1.0**

Date: Wednesday, April 22, 2020 Sheet: 31 of 56

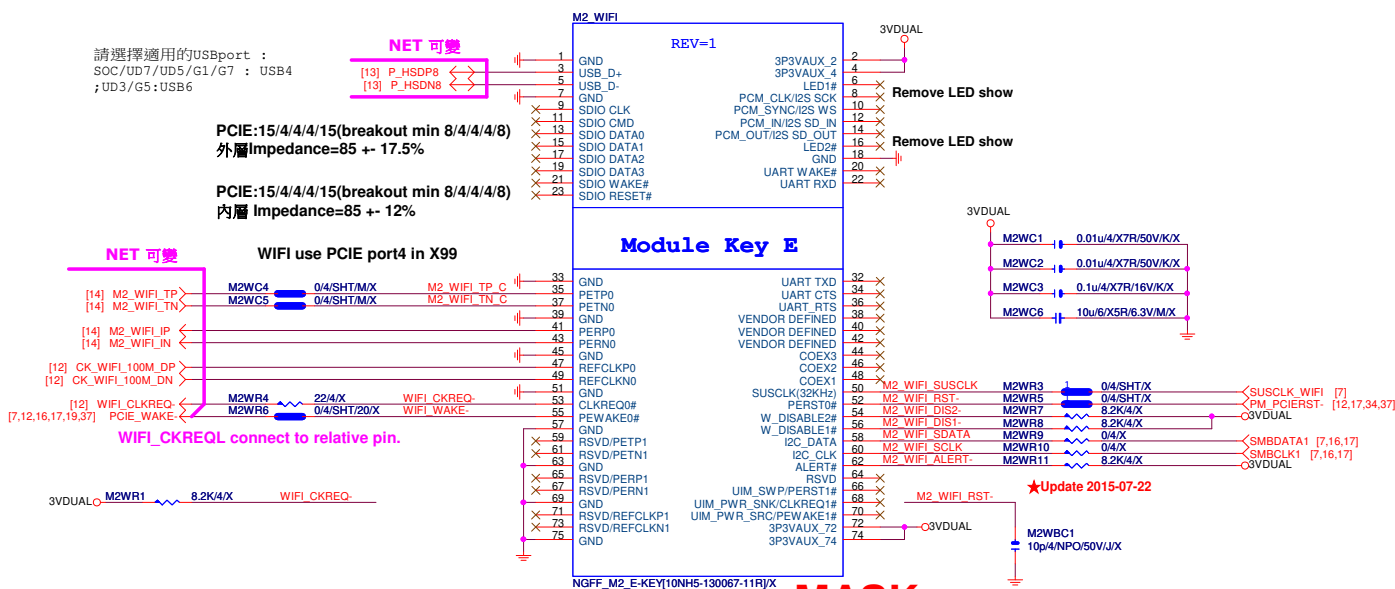
Rev 0.5



GEN4 [有鐵殼] 8.5H鐵殼
Footprint :M2_110(DIP)

Rev: 0.2

FOR M.2 WIFI MODULE @ REAR PANEL

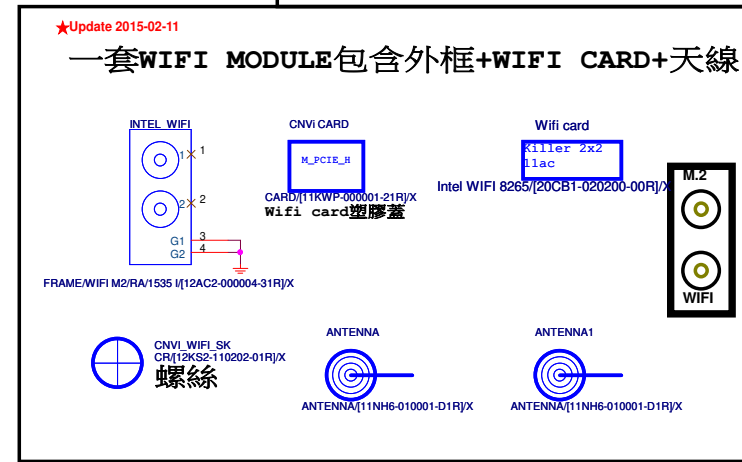


Footprint Notice.

★Update 2015-07-22
★Footprint for
直立式 SMD:
WIFI-EKEY

Footprint Notice.

★Update 2015-07-22
★Footprint for
橫鎖式SMD: NGFF-E-75P-2



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M.2 SOCKET

Size Custom	Document Number B550M AORUS ELITE	Rev 1.0
Date: Monday, May 11, 2020	Sheet 33 of 56	

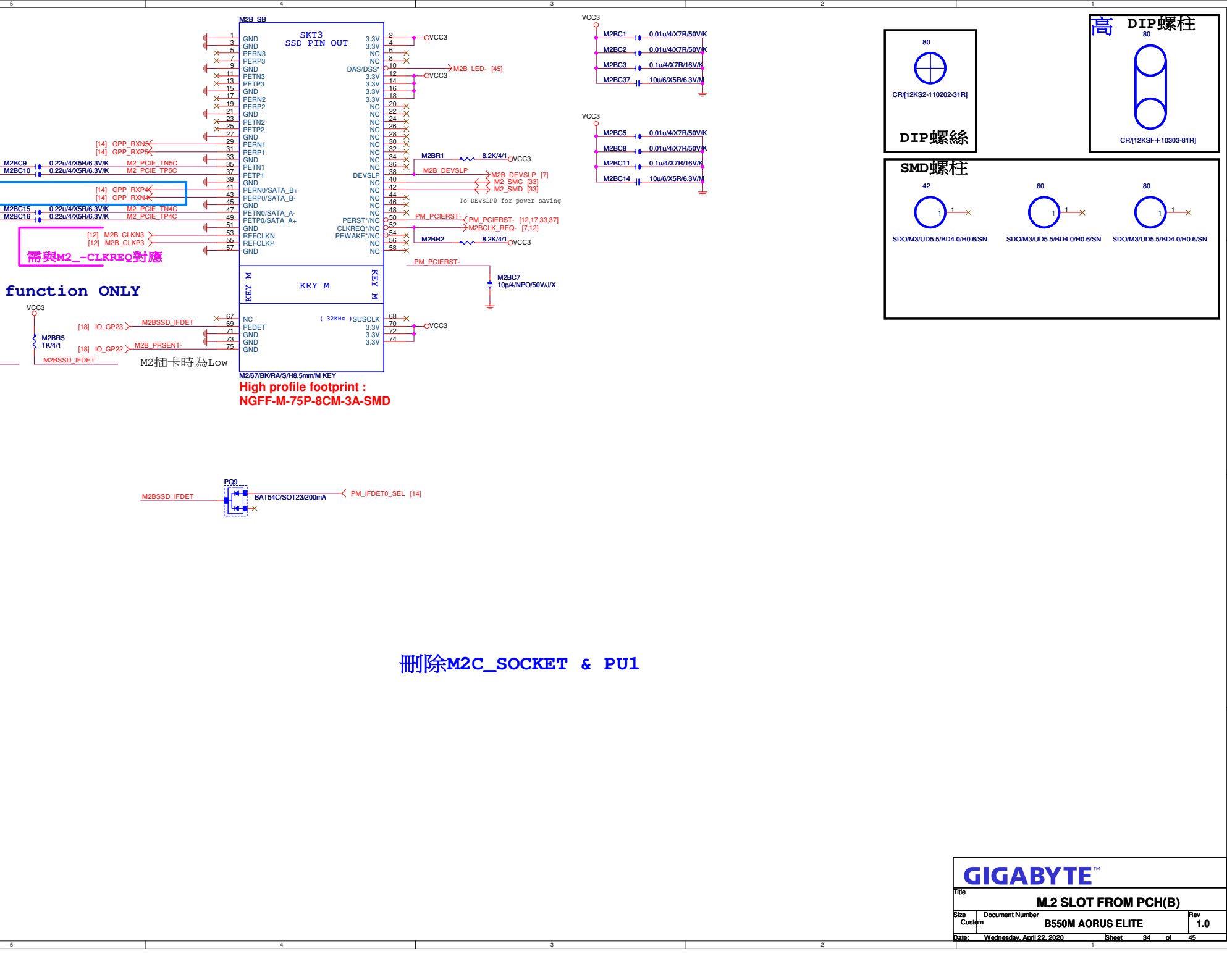


Diagram illustrating the M.2 slot configuration and component placement for the B550M AORUS ELITE motherboard, showing the M.2 slot (M2C_SOCKET) and the M.2 SSD (M2C_SSD) connection.

High profile footprint : NGFF-M-75P-8CM-3A-SMD

需與M2_-CLKREQ對應

function ONLY

刪除M2C_SOCKET & PU1

高 DIP螺柱

DIP螺絲

SMD螺柱

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M.2 SLOT FROM PCH(B)

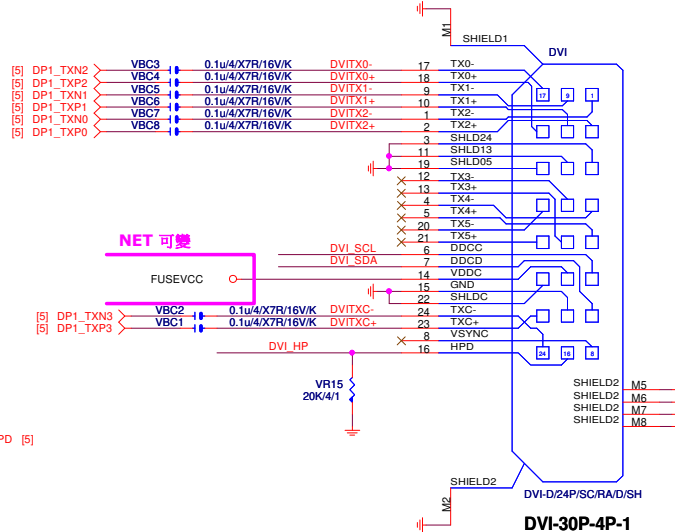
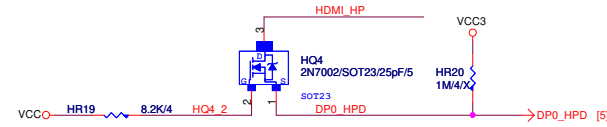
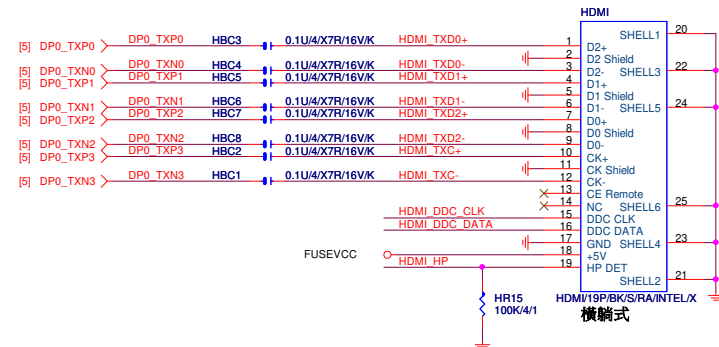
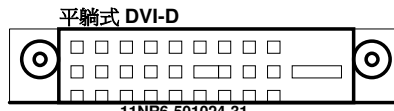
B550M AORUS ELITE

Rev 1.0

Document Number

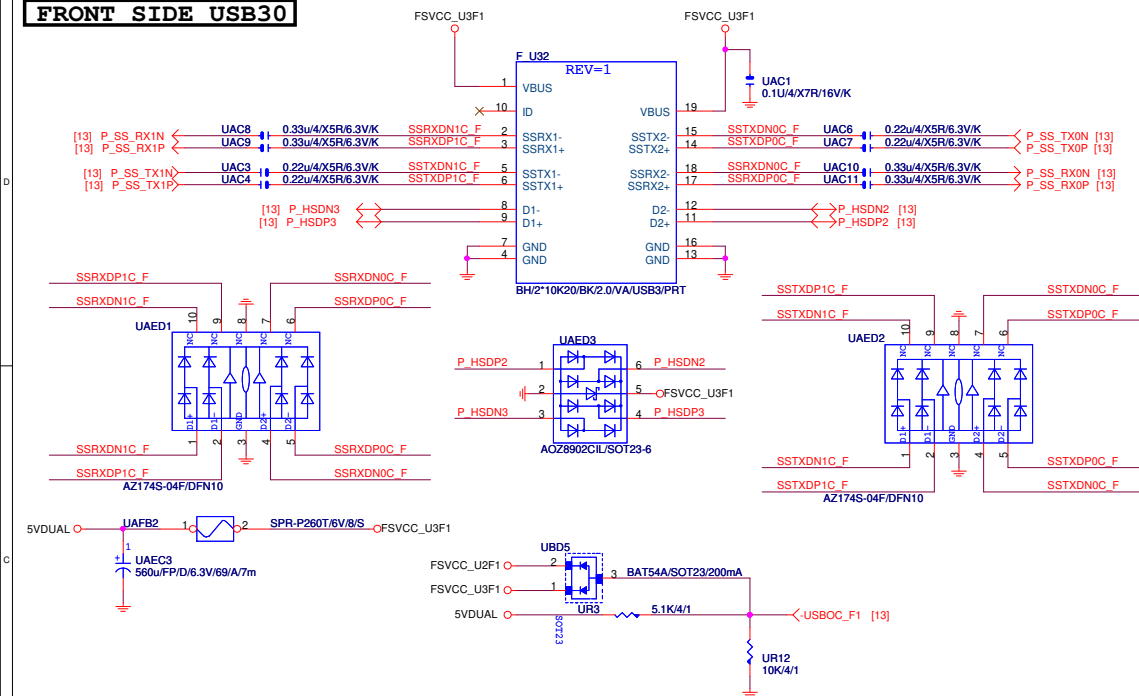
Wednesday, April 22, 2020

Sheet 34 of 45

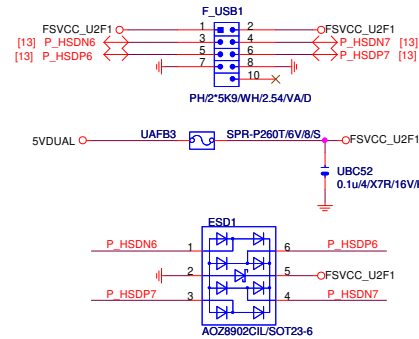
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Title			
KB_USB_DEC PWR			
Size	Document Number	Rev	
Custom	B550M AORUS ELITE	1.0	
Date:	Wednesday, April 22, 2020	Sheet	35 of 56

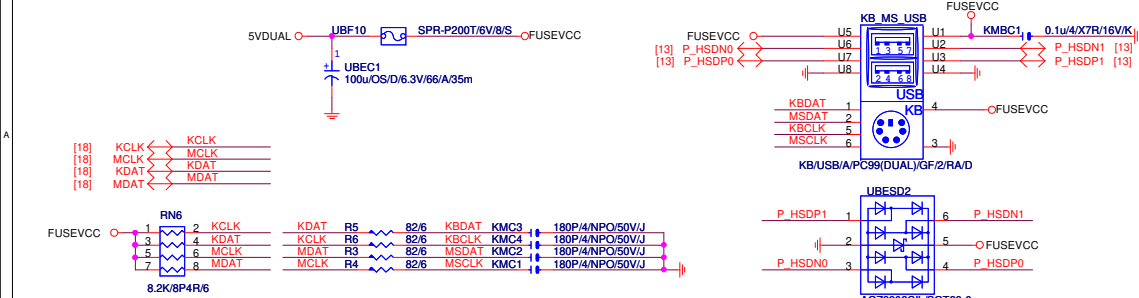
FRONT SIDE USB30



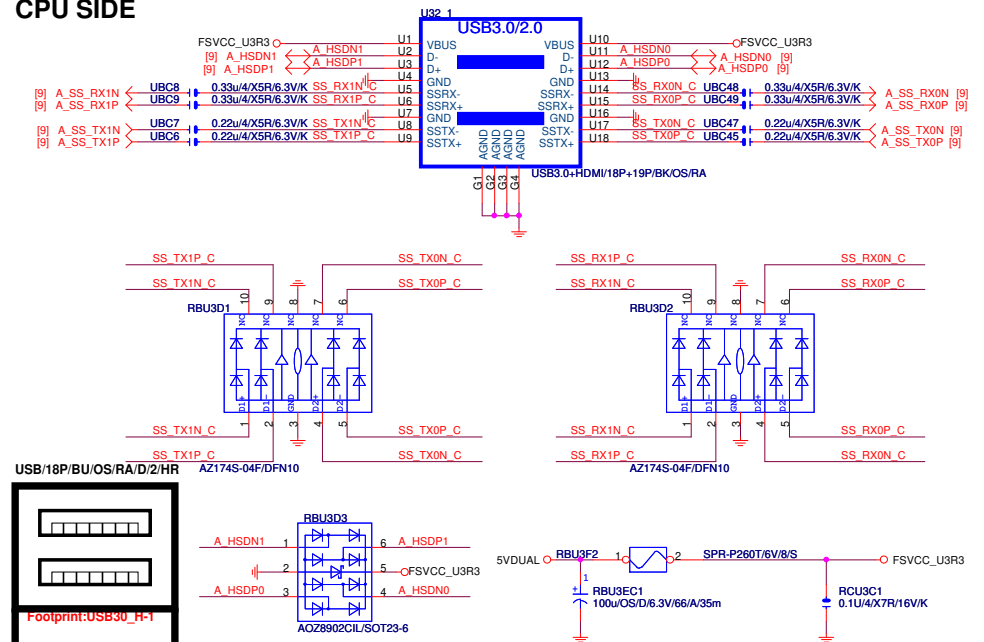
FRONT SIDE USB1



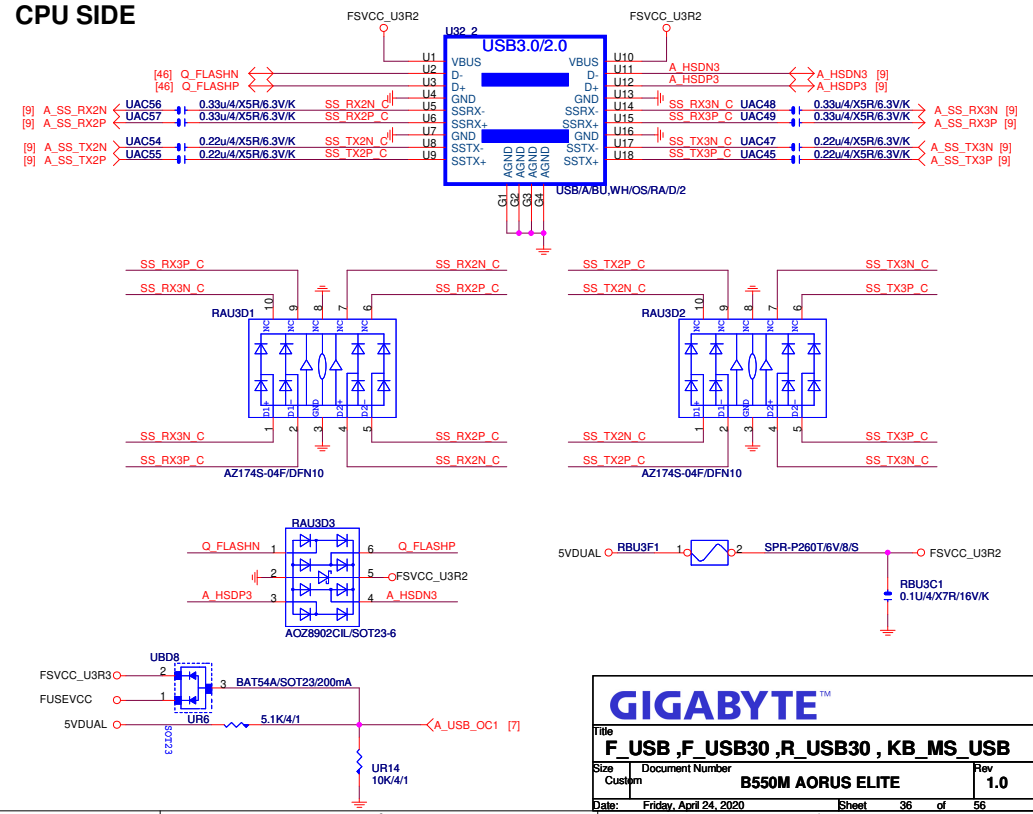
KB/MS & USB



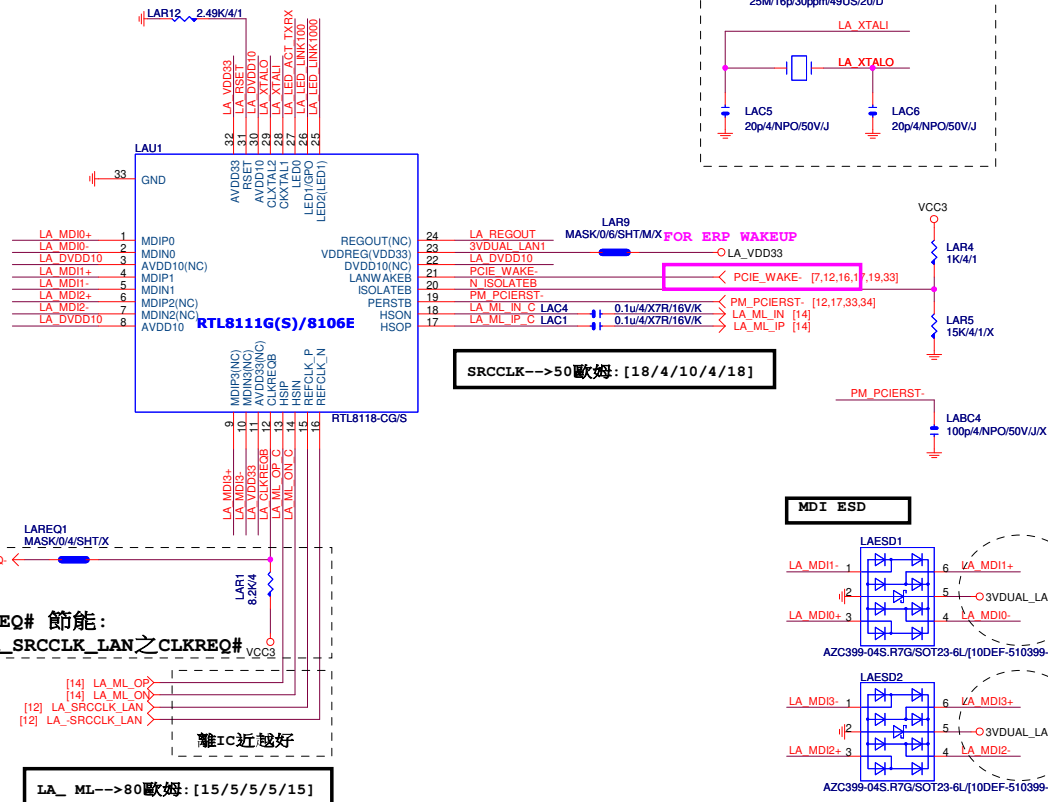
CPU SIDE



CPU SIDE

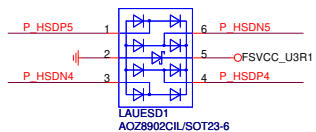


LAN:RTL8111G	R2.03
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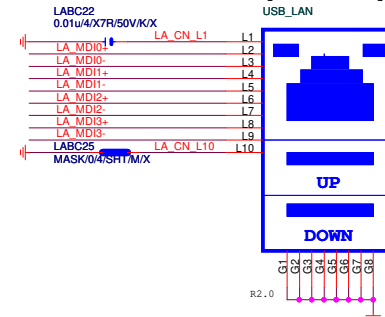


USB_LAN CONNECTOR	R2.03
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RMA ESD PROTECT

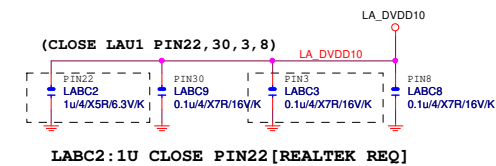


USB_LAN CONNECTOR



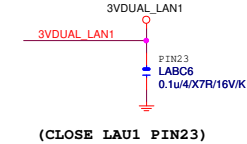
LA_MDI-->100歐姆:[20/4/8/4/20]

LAN POWER

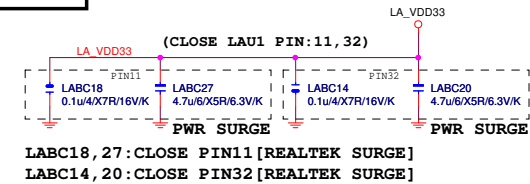


LAN POWER

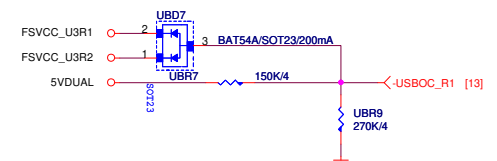
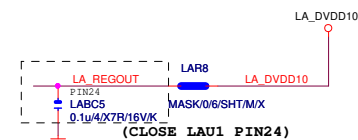
note: lan power連接及電流



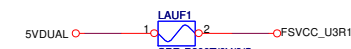
LAN POWER



LAN POWER



USB POWER



Close to connector
USB_LAN 2-Port 2.0A
FUSE-0805

LAN POWER

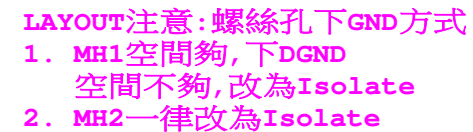


EMI

LAN AGND change GND
Remove Short Pad

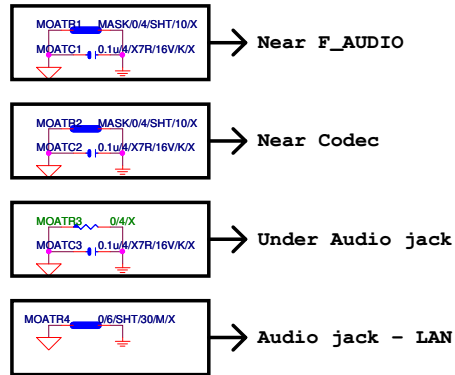
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RTL8111G			
Size	Document Number	Rev	
Custom	B550M AORUS ELITE	1.0	
Date:	Wednesday, April 22, 2020	Sheet	37 of 65



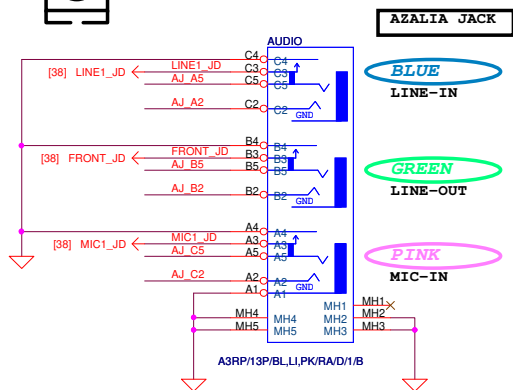
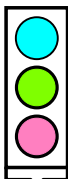
<input type="radio"/> MH1	<input type="radio"/> MH2	
DGND	Isolate	

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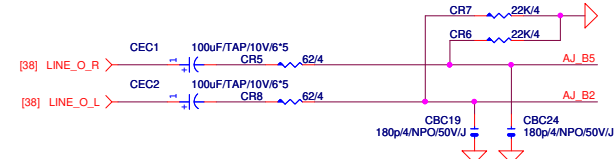


*量産前,0ohm改short pad

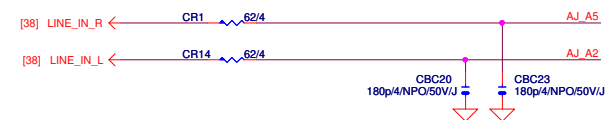
AZALIA JACK



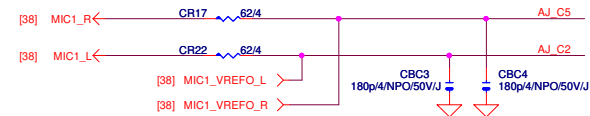
LINE-OUT



LINE-IN



MIC-IN

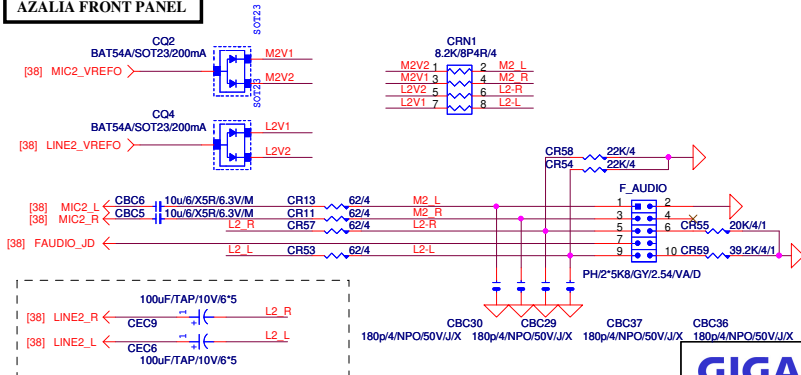


SURROUND

CEN/LFE

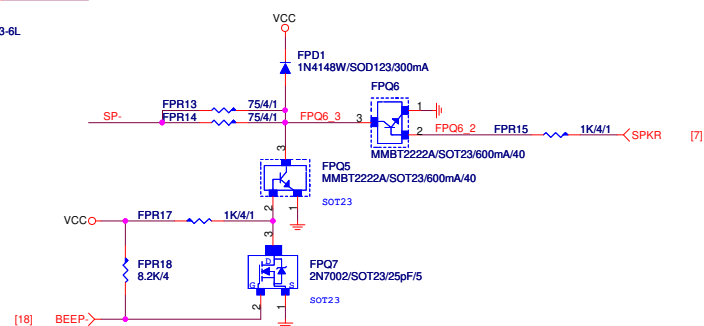
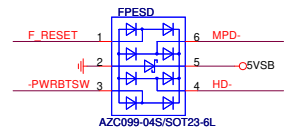
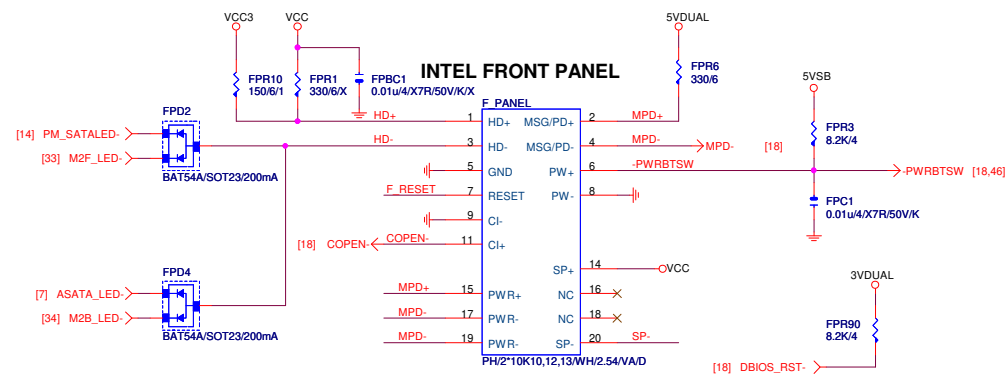
SURR BACK

AZALIA FRONT PANEL

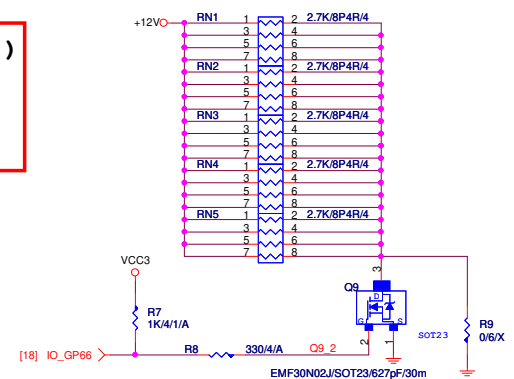
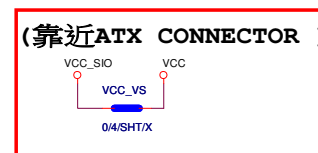
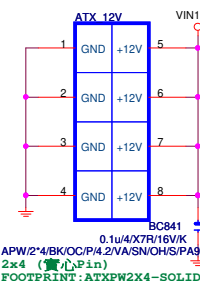
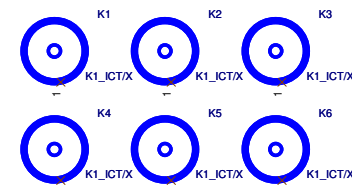
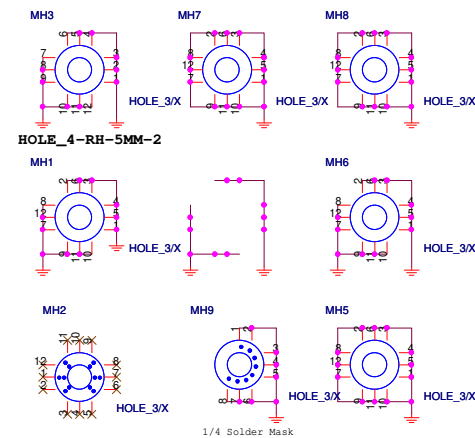
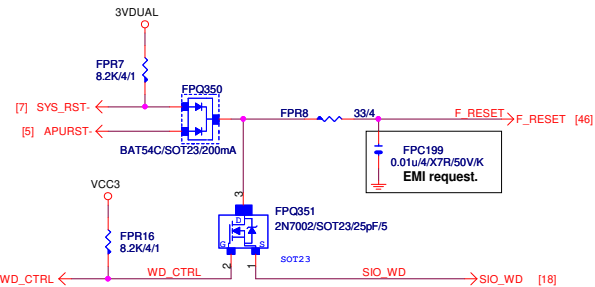
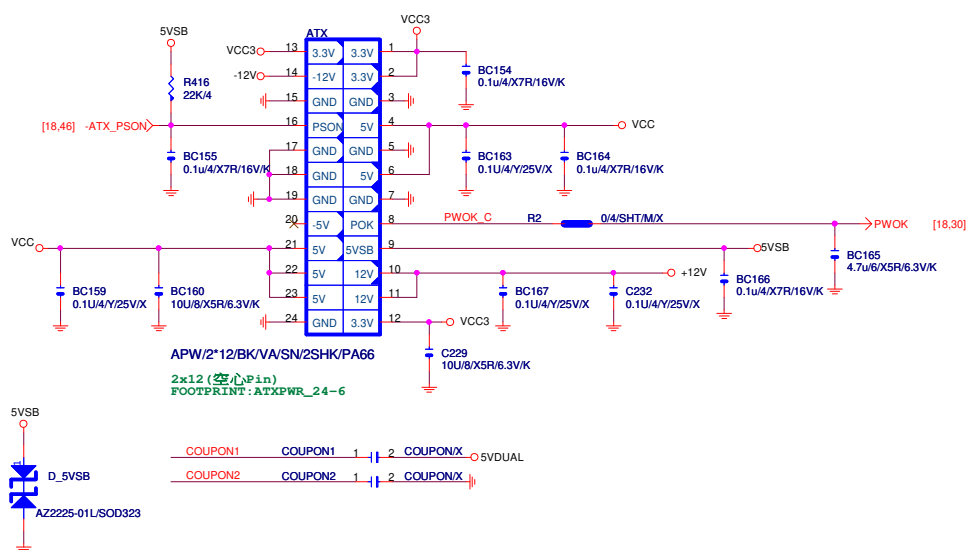


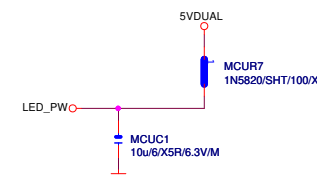
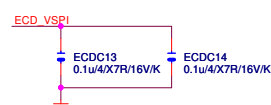
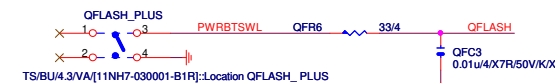
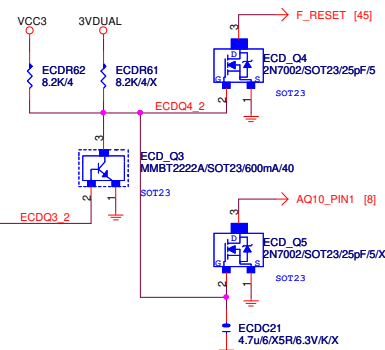
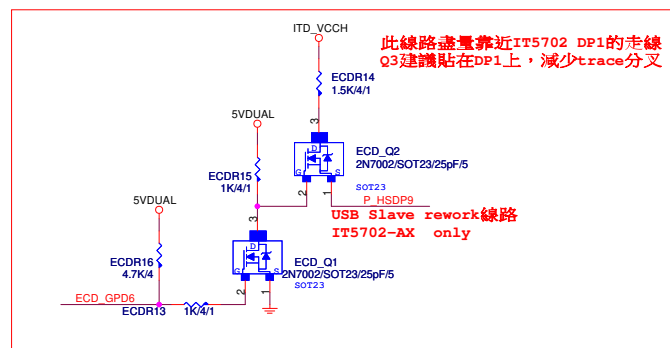
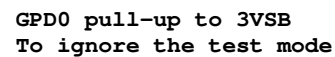
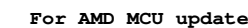
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Title			AUDIO JACK	
Size	Document Number	Rev		
Custom	B550M AORUS ELITE	1.0		
Date:	Wednesday, April 22, 2020	Sheet	39	of 56



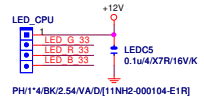
ATX POWER CONNECTOR





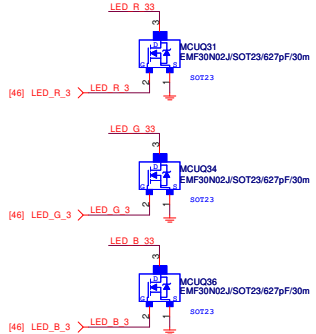
第三區 LED

燈條 LED (LED_CPU放在CPU附近位置)



Footprint "PH1X4-FAN-AMD-L"

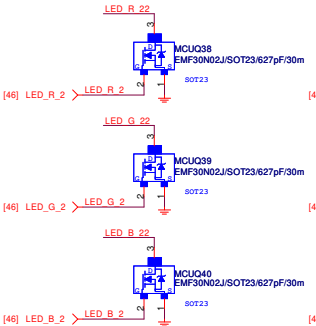
第三區 LED CONTROL



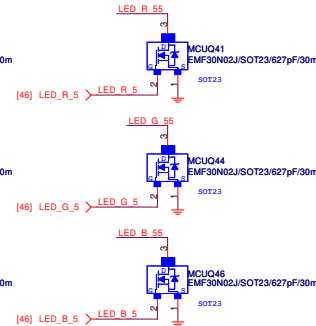
第四區 LED

第五區 LED

第二區 LED CONTROL

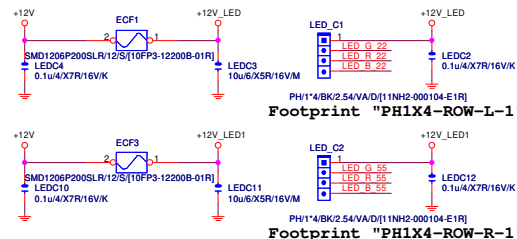


第五區 LED CONTROL



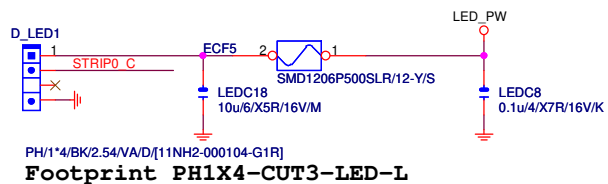
燈條 LED (LED_C1放在PCB左邊板邊位置)

燈條 LED (LED_C2放在PCB右邊板邊位置)



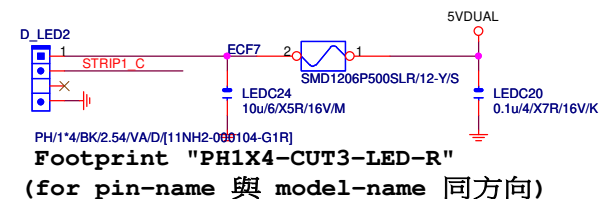
第六區 LED (靠近左上板邊位置)

Digital LED Strip1

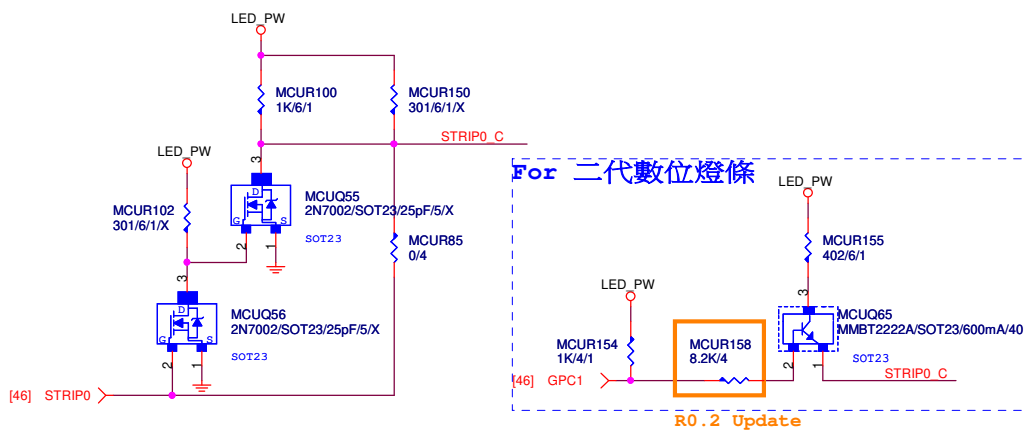


第七區 (靠近右下CPU板邊位置)

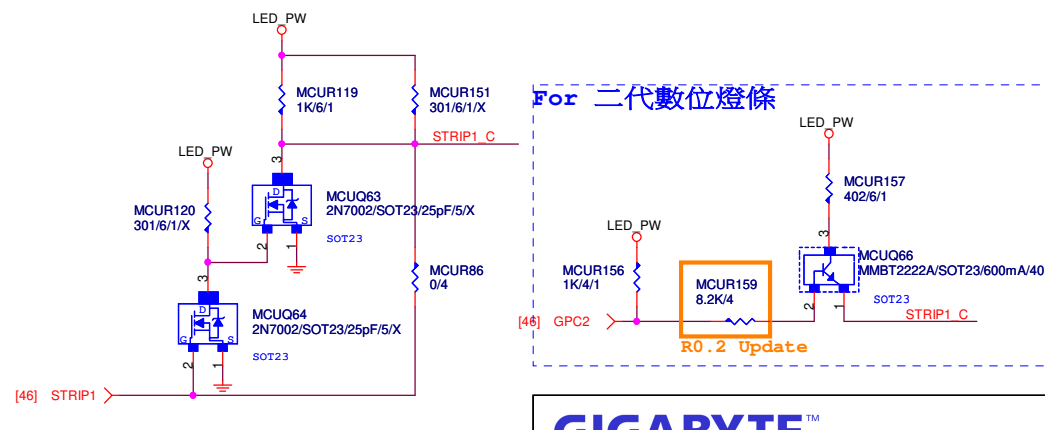
Digital LED Strip2



燈條 Level shift



燈條 Level shift



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Title

D_LED

Size

Document Number

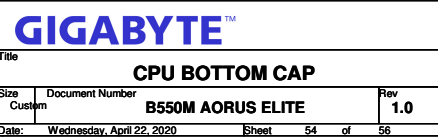
B550M AORUS ELITE

Rev

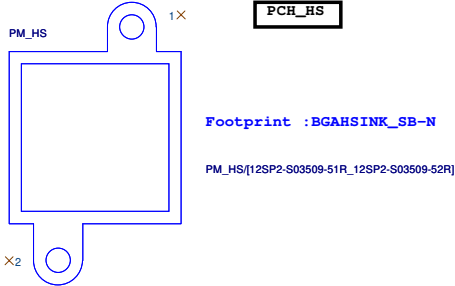
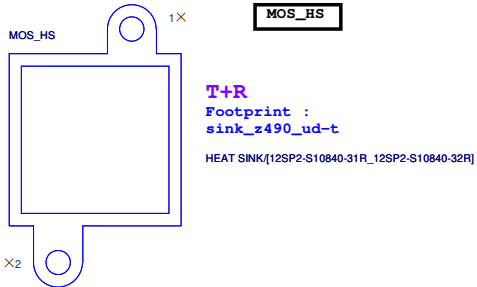
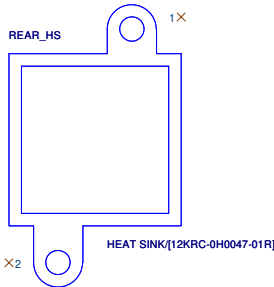
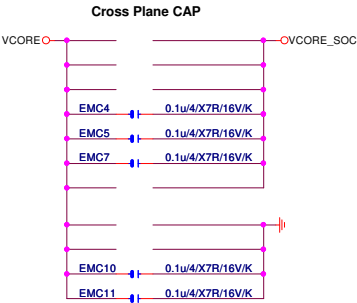
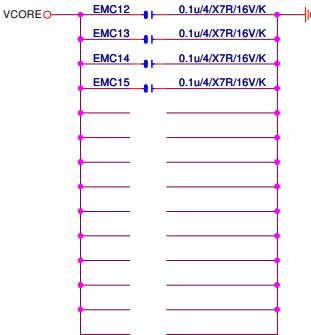
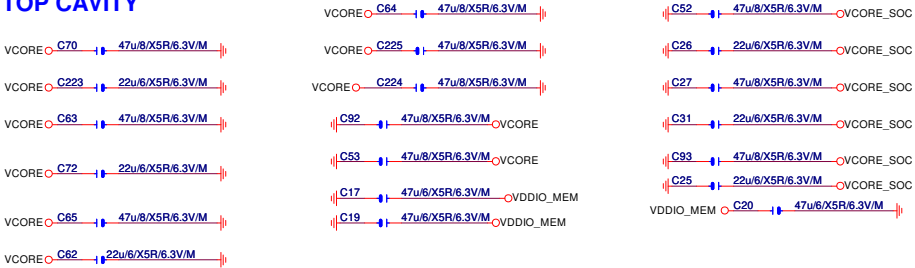
1.0

Date: Wednesday, April 22, 2020

Sheet 46 of 56



CPU TOP CAVITY



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